INTEGRATION, the VLSI journal 55 (2016) 1–11

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Design of a memristor-based look-up table (LUT) for low-energy operation of FPGAs ☆

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ARTICLE INFO

Article history:
Received 17 November 2015
Received in revised form
23 February 2016
Accepted 23 February 2016
Available online 2 March 2016

Keywords:
Memristor
Non-volatile memory
Sneak path
FPGA
LUT

ABSTRACT

This paper presents a scheme for designing a memristor-based look-up table (LUT) in which the memristors are connected in rows and columns. As the columns are isolated, the states of the unselected memristors in the proposed scheme are not affected by the WRITE/READ operations; therefore, the prevalent problems associated with nanocrossbars (such as the write half-select and the sneak path currents) are not encountered. Extensive simulation results of the proposed scheme are presented with respect to the WRITE and READ operations; its performance is compared with previous LUT schemes using memristors as well as SRAMs. It is shown that the proposed scheme is significantly better in terms of WRITE time and energy dissipation for both memory operations (i.e. WRITE and READ); moreover it is shown that the READ delay is nearly independent of the LUT dimension. Simulation using benchmark circuits for FPGA implementation show that the proposed LUT offers significant improvements also at this level.

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1. Introduction

Field Programmable Gate Arrays (FPGA) have been widely utilized because they allow the fast hardware design and realization of digital systems at relatively low development cost and good performance [1]. The general scheme of an FPGA consists of configurable resources; among them, Look Up Tables (LUT) are used to implement combinational logic circuits [2]. All configurable resources (inclusive of the LUTs) are controlled through the configuration bits stored in Static Random Access Memories (SRAMs) [2]. SRAM-based FPGAs are volatile, so unable to retain the configuration bits when a power loss occurs. Non-Volatile (NV) flash memories are utilized as alternative to store the configuration bits [3]; this technology requires a larger area, higher costs [4], high delay for retrieving the configuration bits and a substantial increase of leakage current in stand-by mode [5] (so causing additional power dissipation). Hence to overcome the above mentioned issues, NV memories (for LUT operation) made of so-called resistive elements (such as the memristor) have been proposed as storage elements. Memristor-based memories using nanocrossbars have been extensively analyzed in the technical literature [8,9,11–17].

These memories have been advocated as a potential replacement for conventional NV Flash Memories (NVFMs) as LUTs in a FPGA due to the higher density and lower power consumption [8]. However, these memories usually use nanocrossbars, whose operation is affected by sneak path currents and the write half-select [13], i.e. following few WRITE/READ operations, the memristances of the unselected memristors change, causing errors in stored data.

To address these issues, this paper proposes a novel scheme in which the memristors are connected in rows and columns, but the columns are isolated. It is then possible to prevent the sneak path current and write half-select problems, because the memristances of the unselected memristors are unaffected. Also the proposed scheme retains the advantages of [16], such as no power dissipation in stand-by mode; no refresh pulse and no $V/2$ bias are required (so also lowering the number of power rails). The LUT scheme presented in this paper does not use a nanocrossbar while still retaining the same advantages of previous approaches, for example the utilization of WRITE and READ schemes of [16] for improved performance. Extensive simulation results and a detailed comparative analysis (inclusive of circuit modeling) with previous works [11,12,16] show that the proposed scheme is significantly better in terms of WRITE time and energy dissipation for both the WRITE and READ operations. Simulation is also extended from circuit-level to FPGA-level; a FPGA implementation using the proposed LUT shows significant improvement in performance (delay and energy) compared to both

☆This manuscript is an extended version of [19] by the same authors.

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http://dx.doi.org/10.1016/j.vlsi.2016.02.005
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SRAM-based and existing memristor-based (non-volatile) schemes, thus confirming its viability.

2. Review and preliminaries

2.1. Memristor

The four circuit variables that define circuit theory, are charge, flux, current and voltage; these four variables account for the six possible (two-variable) combinations, out of which only five of them (as relations) are known and well understood. Chua theorized this fourth fundamental element in 1971 [6] and named it *memristor*. The memristor is characterized by its *memristance function* given by the ratio of the change of flux to the change of charge. HP Lab has achieved the first physical realization of a memristor using a titanium dioxide film sandwiched between two platinum electrodes [7]. In the HP implementation, there are two layers of film; one has a slight depletion of oxygen atoms while the other layer is non-depleted. The oxygen vacancies act as charge carriers, i.e. the depleted layer has a significantly lower resistance than the non-depleted layer. When an electric field is applied, the oxygen vacancies drift in the direction of the field, changing the boundary between the high-resistance and low-resistance layers. The application of a positive voltage at one end moves the oxygen ions to the other end of the film, thereby shifting the boundary between the doped and undoped film regions; the application of a voltage with opposite polarity reverses this phenomenon.

Let $w(t)$ denote the length of the doped region (as function of time) and D the total length of the titanium dioxide layer (memristor). Then $w(t)/D$ is referred to as the Normalized State Parameter (NSP) [17]. When $w(t)=D$, then NSP$=1$ and the memristor is at the least resistance value (R_{ON}), i.e. the oxygen ions spread over the entire film. If $w(t)=0$ then, NSP$=0$ and the memristor is at the highest resistance value (R_{OFF}), i.e. no doped region is present. The value over which the resistance varies from R_{ON} to R_{OFF} is defined as the so-called *range of the memristor*. The threshold value of the NSP is the value that allows to correctly distinguish the binary values (0, 1) of the stored data; this is assumed to be 0.5. An updated version of the model in [18] is utilized in this paper because it has shown close resemblance to the HP Labs implementation [7]. Moreover, throughout this manuscript unless specified, the default values of the parameters are given as follows: Memristor: $R_{ON}=100\ \Omega$; $R_{OFF}=19\ k\Omega$, $D=10$ nm; Transistors: Low Power (LP) model of the Predictive Technology Model (PTM) [20], gate length$=32$ nm and aspect ratio of 2; the on-state and off state resistances of transistors $T1$ and $T2$ are 5.552 kΩ and 348.22 GΩ respectively; accuracy of NSP: 0.1%; Simulator: LTSPICE IV.

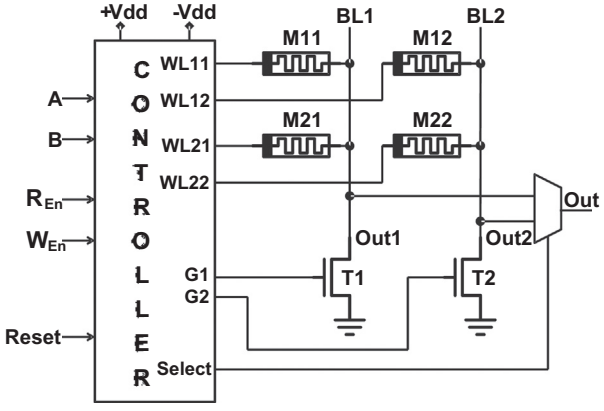

Fig. 1. Proposed new scheme for a two-input LUT memory block implemented using memristors.

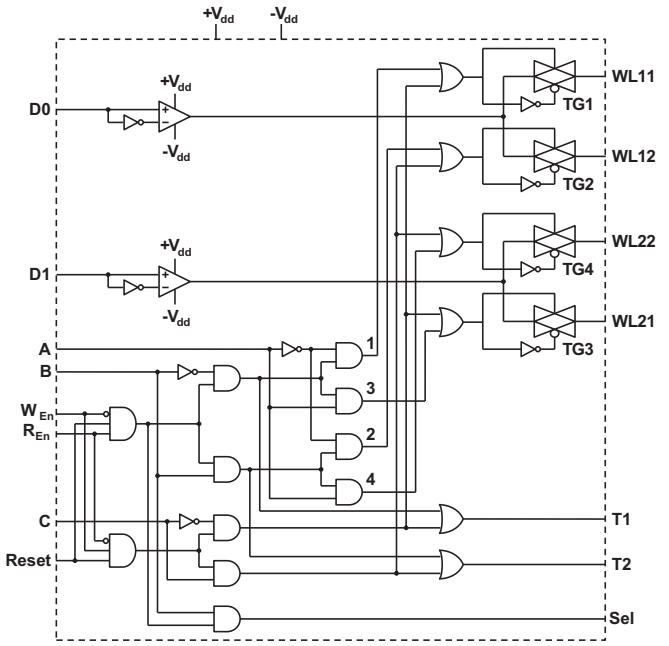

Fig. 2. Circuit diagram of the controller for a two-input LUT.

Table 1
Voltage requirements for the WRITE operation of M11 and M21 and READ operations on M11 using the proposed LUT.

	WL11	WL12	WL21	WL22	BL1 voltage	BL2 voltage
Write 1	V_{dd}	*Floating*	V_{dd}	*Floating*	*GND*	*Floating*
Write 0	$-V_{dd}$	*Floating*	$-V_{dd}$	*Floating*	*GND*	*Floating*
Read	$\pm V_{dd}$	*Floating*	*Floating*	*Floating*	*GND*	*Floating*

Table 2
WRITE and READ operations using proposed scheme.

Operation	R_{En}	W_{En}	C	A	B	T1	T2	M11 (1) (00)	M12 (2) (01)	M21 (3) (10)	M22 (4) (11)
Write	↓	↑	0	×	×	↑	↓	D0	z	D1	z
	↓	↑	1	×	×	↓	↑	z	D0	z	D1
Read	↑	↓	×	0	0	↑	↓	D0	z	z	z
	↑	↓	×	0	1	↓	↑	z	D0	z	z
	↑	↓	×	1	0	↑	↓	z	z	D1	z
	↑	↓	×	1	1	↓	↑	z	z	z	D1

Note: ↓ – Low; ↑ – High; × – don't care; z – floating (high resistance).

2.2. Non-volatile memory schemes

The memristor is a potential candidate for replacing SRAM and NVFM [13] for storing the configuration bits of an FPGA. In recent years, new schemes have been proposed for FPGAs by using memristor based memories [8–17]. A novel interconnect design for FPGAs has been proposed using only memristors and metal wires [8,9]; an hybrid design using SRAMs and memristors to implement the Non-Volatile LUT (NVLUT) of a FPGA has been reported in [10]. In addition to the NV feature, this NVLUT reduces power dissipation in the stand-by mode. However it suffers from an increase in dynamic power dissipation, area and delay. [13] has presented a

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