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Multi-mode parallel and folded VLSI architectures for 1D-fast Fourier transform

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ABSTRACT

The modern real time applications like orthogonal frequency division multiplexing and etc., demand high performance fast Fourier transform (FFT) design with less area and clock cycles. This paper proposes efficient FFT VLSI architectures using folded/parallel implementation. In the proposed folded FFT architecture, the number of cycles required to complete the operation is less than single path delay feedback (SDF)/multi-path delay commutator (MDC) architectures. In the proposed parallel FFT architecture, N-point FFT is implemented by using one $N/2$-point FFT without much extra hardware. Both the proposed architectures are implemented for radix-2, 2^2, and 4 using 45 nm technology library. The proposed parallel architecture achieves 56.7% and 40.6% of area reduction as compared with the existing parallel architecture based 16-point radix-2 and radix-2^2 DIF FFTs respectively. The proposed folded architecture achieves 65.5%, 51.1%, and 35.8% of worst path delay reduction as compared with the existing SDF based 16-point radix-2, radix-2^2, and radix-4 DIF FFTs respectively.

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1. Introduction

FFT [1] is the most popular algorithm used in digital signal processing applications like orthogonal frequency division multiplexing (OFDM) [2,3], ultra wide band (UWB) [4], and etc. In general, VLSI architecture for any digital signal processing application is classified into two categories; they are (1) parallel form and (2) folded form [5]. The main difference between the parallel and folded architectures is the number of clock cycles and area. In parallel architecture, total area is greater than folded. In folded architecture, the number of clock cycles is greater than parallel. Therefore, parallel architecture can be used in the applications, where time optimization (high throughput) is the primary goal (Example – Super Computer). Similarly, folded architecture can be used in some applications, where area optimization is the primary goal (Example – Handheld devices). Usually, this kind of parallel/folded architectures is used in digital filter design, discrete transformation and etc. The radix-2, 2^2, and 4 parallel FFT architectures are explained in [7–9], respectively. The folded FFT architectures are further classified into single path delay feedback (SDF), single path delay commutator (SDC), multi-path delay feedback (MDF), and multi-path delay commutator (MDC). The objective of FFT is to reduce time complexity of discrete Fourier transform (DFT) [10].

Eq. (1) shows the basic operation of DFT.

$$W_{N/2}^{r} = e^{-j2\pi nr/(N/2)}$$

$$X[r] = \sum_{n=0}^{N-1} x[n]e^{-j2\pi nr/N}; \quad r = 0, 1, \ldots, N-1 \tag{1}$$

$$X[2r] = \sum_{n=0}^{N/2-1} (x[n]+x[n+N/2])W_{N/2}^{r}; \tag{2}$$

where $r = 0, 1, \ldots (N/2)-1$

$$X[2r+1] = \sum_{n=0}^{N/2-1} (x[n]-x[n+N/2])e^{-j2\pi/Nn}W_{N/2}^{r}; \tag{3}$$

where $r = 0, 1, \ldots (N/2)-1$.

Eqs. (2) and (3) show decompositions in radix-2 decimation in frequency (DIF) FFT. Radix-2 16-point single path delay feedback (SDF) [11] DIF FFT architecture is shown in Fig. 1(a). Here the Butterfly units are represented as $BF1$, $BF2$, $BF3$, and $BF4$. Each Butterfly output is multiplied with corresponding twiddle factor from the multiplexer. The twiddle factor is represented as $W_N{}^k$ and which is equal to $e^{-j2\pi nk/N}$. The twiddle factors can be selected by the appropriate select lines se_1, se_2, and se_3. Throughout this paper, registers are represented as shaded square boxes. Similarly, the notation z^{-N_1} is used to represent N_1 number of cascaded hardware registers which are used for delay. During each clock cycle, only one set of inputs can be processed by every Butterfly unit. Eqs. (4) and (5) show the variables used to derive the radix-2^2

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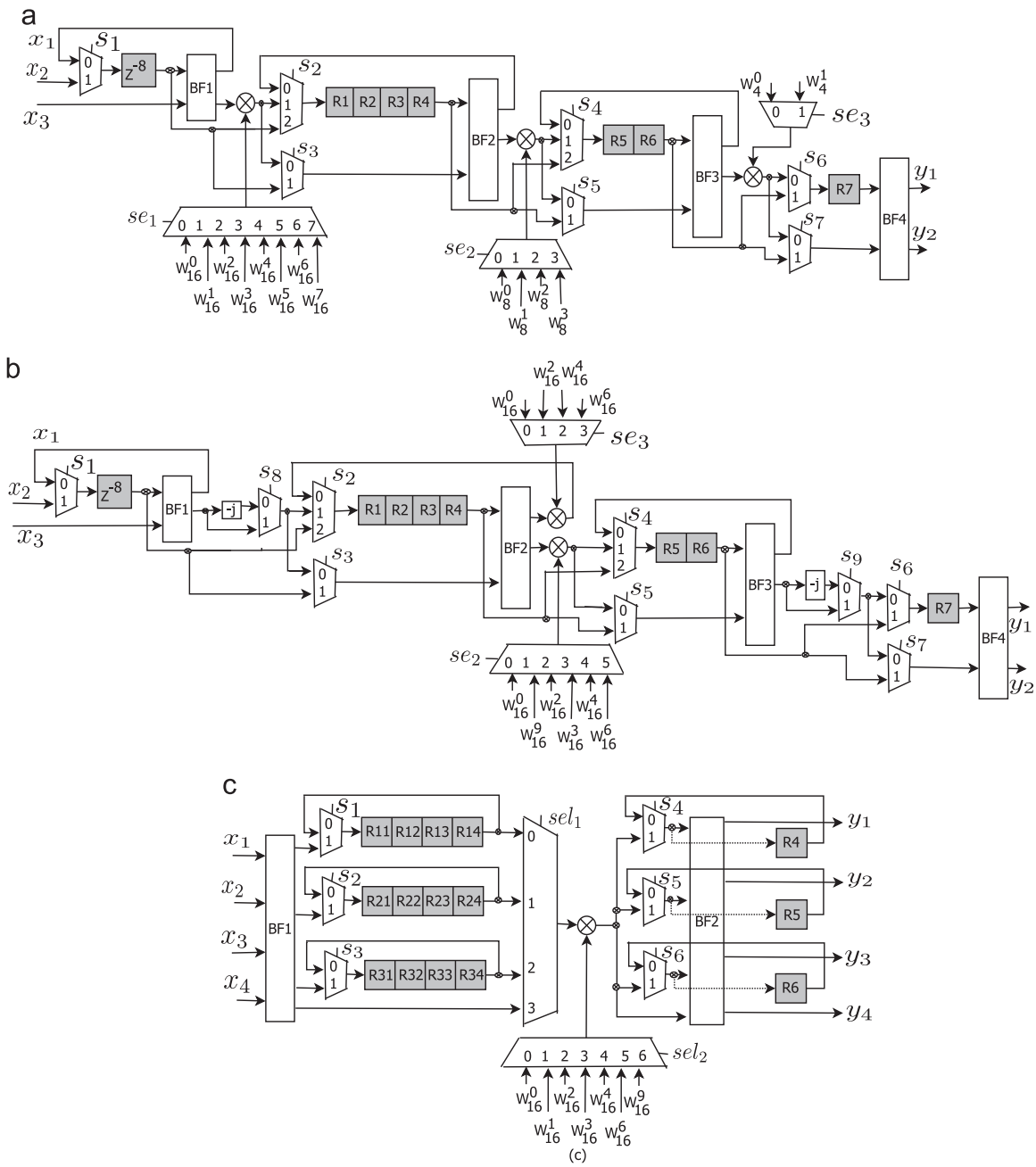

Fig. 1. 16-point single path delay feedback DIF FFT using (a) Radix-2, (b) Radix-2^2, and (c) Radix-4 implementation.

FFT algorithm which is shown in the equations from (6) to (10).

$$n = \left\langle \frac{N}{2}n_1 + \frac{N}{4}n_2 + n_3 \right\rangle N \tag{4}$$

$$k = \langle k_1 + 2k_2 + 4k_3 \rangle N \tag{5}$$

$$X(k_1+2k_2+4k_3) = \sum_{n_3=0}^{(N/4)-1} \sum_{n_2=0}^{1} \sum_{n_1=0}^{1} x\left(\frac{N}{2}n_1 + \frac{N}{4}n_2 + n_3\right) W_N^{nk} \tag{6}$$

$$W_N^{nk} = (-j)^{n_2(k_1+2k_2)} W_N^{n_3(k_1+2k_2)} W_N^{4n_3k_3} \tag{7}$$

$$X(k_1+2k_2+4k_3) = \sum_{n_3=0}^{(N/4)-1} [H_{N/4}(n_3,k_1,k_2)] W_N^{n_3(k_1+2k_2)} W_{\frac{N}{4}}^{n_3k_3} \tag{8}$$

$$H_{\frac{N}{4}}(n_3,k_1,k_2) = B_{\frac{N}{2}}(k_3,k_1) + (-j)^{(k_1+2k_2)} B_{\frac{N}{2}}\left(n_3 + \frac{N}{4}, k_1\right) \tag{9}$$

$$B_{\frac{N}{2}}(n_3,k_1) = x(n_3) + (-1)^{k_1} x\left(n_3 + \frac{N}{2}\right) \tag{10}$$

Radix-2^2 16-point single path delay feedback [12,14] DIF FFT is shown in Fig. 1(b). Here, the second Butterfly unit ($BF2$) contains two complex number multipliers. The output from first and third Butterfly units is multiplied by $(-j)$. The Radix-2^2 16-point SDF FFT operation can follow Fig. 1(a). Eqs. (11)–(16) show radix-4 DIF FFT algorithm, where $y(n)$, $y(n+\frac{N}{4})$, $y(n+\frac{2N}{4})$, and $y(n+\frac{3N}{4})$ are radix-4 $\frac{N}{4}$-point DIF FFT of $X(4k)$, $X(4k+1)$, $X(4k+2)$, and $X(4k+3)$ respectively.

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