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Γ (Gamma): A SaaS-enabled fast and accurate analog design System



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ABSTRACT

With ever increasing demand for lower power consumption, lower cost, and higher performance, designing analog circuits to meet design specifications has become an increasing challenging task. Analog circuit designers must, on one hand, have intimate knowledge about the underlining silicon process technology's capability to achieve the desired specifications. They must, on the other hand, understand the impact of tweaking circuits to satisfy a given specification on all circuit performance parameters. Analog designers have traditionally learned to tackle design problems with numerous circuit simulations using accurate circuit simulators such as SPICE, and have increasingly relied on trial-and-error approaches to reach a converging point. However, the increased complexity with each generation of silicon technology and high dimensionality of searching for solutions, even for some simple analog circuits, have made the trial-and-error approach extremely inefficient, causing long design cycles and often missed deadlines. Novel rapid and accurate circuit evaluation methods that are tightly integrated with circuit search and optimization methods are needed to aid design productivity.

Furthermore, the current design environment with fully distributed licensing and supporting structures is cumbersome at best to allow efficient and up-to-date support for design engineers. With increasing support and licensing costs, fewer and fewer design centers can afford it. Cloud-based software as a service (SaaS) model provides new opportunities for CAD applications. It enables immediate software delivery and update to customers at very low cost. SaaS tools benefit from fast feedback and sharing channels between users and developers and run on hardware resources tailored and provided for them by the software vendor. On the downside, web-based tools are expected to perform in a very short turn-around schedule and be always responsive.

This paper presents a list of innovations that come together to a new class of analog design tools: 1). Lookup table-based approach (LUT) to model complex transistor behavior provides both the necessary accuracy and speed essential for repeated circuit evaluations. 2). The proposed system architecture tight integrate the novel LUT approach with novel system level functions to allow further significantly better accuracy/speed tradeoff and faster design convergence with designer's intent. 3). Incorporating use inputs at key junctures of the design process allows the tool to better capture designer's intent and improve design convergence. 4). The combination of high accuracy and faster evaluation time make it possible to incorporate SaaS features, such as short solution space navigation steps and crowdsourcing, into the tool. This allows sharing of server-side resources between many users. Instead of fully automating a signoff circuit optimization process, the proposed tool provides effective aid to analog circuit designers with a dash-board control of many important circuit parameters with several orders faster in computation time than SPICE simulations.

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1. Introduction

Analog circuit design automation has been lagging significantly behind its digital counterpart. The main reason for this is the complexity of evaluating circuits against users' specifications and a large number of competing design goals in the optimization

process. Since the 1980s, several software research projects attempted to improve design productivity and even provide fully automated synthesis of analog circuits [1–4]. Most did not mature beyond academic prototypes. Some made it into market and attracted customers [5], but did not scale up to complex topologies and failed to migrate along each generation of silicon technology [6]. Yet, demand for lower power consumption, lower cost, and higher performance for analog circuits is increasing. Consequently,

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designing analog circuits to meet tight specifications has become an increasing challenging task. The need for practical solutions to improve design productivity is ever present in the semiconductor industry, where time-to-market project constraints push the analog design efforts closer to a bottleneck position.

The majority of the existing tools have the following characteristics in common:

1. They start with a topology plus performance constraints and attempt to generate production-ready circuit autonomously without any designer feedback in the loop.
2. They use internal or enwrapped simulations to evaluate solutions during the optimization process.
3. They run “on premises”, as opposed to hosted remotely, requiring customers to provide the hardware and sometime complementary software.

To circuit designers, the existing tools and approaches can be viewed as black-box approaches. The black-box-type optimization has several disadvantages:

1. For approaches using the SPICE engine for their performance evaluations, it typically takes long time to completion, breaking the natural flow of users' decision making process.
2. For approaches using high-level algebraic formula for their performance evaluations, the results are typically far from desired optima due to tool's inabilities of capturing circuit's high order effects with even complex algebraic formula.
3. Users often have to constrain the design problem well and be vigilant about the tasks they hand-over to the machine, because of the high risk of starting a long run that ends with results that are outside the constraint region.
4. The internal optimization process in the flow does not allow designer feedback. Users complain that the pre-defined optimization flow is useful in solving high volume of problems in correct, consistent and repeatable process (e.g. ASIC place and route), but designers often reach better and faster solutions when presented with one at a time instances of more complex problem, such as analog circuit design.

In existing attempts, tool programmers make a common mistake of putting the machine at the center of the flow by prioritizing functional features [7] and failing to give users the control to run optimization steps and stages interactively and intuitively, which is crucial in analog circuit design process as the number of competing design goals are often too numerous for any algorithm to handle successfully. Instead, users are kept out of the loop once the optimization process has started and then are given the choice of accepting the final result or re-spin it, if those are not satisfactory. Conversely, web-based tools do not have the luxury of running hours-long processes of A-Z optimization flow. Commonly accepted expectations from internet responsiveness [8] dictate much faster turn-around, continuous controllability and intuitive, dynamic visualization of runs in progress. These challenging expectations can also be opportunities for a new class of analog design tools that put designers back at the helm of the design flow. Web application for sizing transistors and designing analog circuits must focus on the least computationally-ambitious atomic tasks and allow users to navigate between them and connect the flow. One aspect of design automation that can be a good fit for the web is mapping and visualizing solution spaces of topologies and specs to provide users with performance trade-off they need to make engineering decisions.

Stand-alone or tool-integrated SPICE simulations decouple the task of evaluating circuits from the optimization engine. The biggest benefit of using generic SPICE is that technology-specific parameters

and models [9] can be integrated and modified with foundry characterized behavior with little tool vendor involvement. However, the silicon-accurate results provided by SPICE come at a cost. Evaluations of reasonably sized analog circuits include overheads, such as topology analysis, redundant calculations of transistor physical characteristics and simulations of elaborate test harnesses, necessary to adapt circuit property measurements to one of the generalized simulation types: DC, AC and Trans. The amount of overhead can make the repeated evaluations required during analog circuit design and tradeoffs extremely inefficient. This impact can be even worse for analog circuit design tools in the SaaS environment where a large number of circuits need to be evaluated during a typical HTTP transaction interval.

On-premises software is a common feature to most contemporary industrial EDA software. High demand in computational resources makes tool vendor focus on software alone, leaving the customer to provide their own hardware. The complexity and diversity of applications gave birth to the classic EDA support structure. Tools are coded by EDA vendors with a vast range of algorithms and configurations. The task of choosing between all the configurations is passed to the responsibility of customers, who are left to figure out best usage of input scripts, configuration files and GUI's. Vendors have to employ an army of field applications engineers (FAE) to help customers figure out the best configuration and keep the vendor itself up to date with the market needs. An FAE, like the software itself, is most often embedded on premises with the design team. This semi-automation structure is expensive and cumbersome. Effective SaaS systems attempt to implement crowd-sourced feature additions, peer networking and remote help forums to eliminate the need for human-based support structure. Direct communication channel can improve tool performance with automatically collected usage statistics. Certain results can be shared and reused between customers in a behind the scenes automated learning and archiving system. New features, conceived automatically from public-demand chats and surveys, are available instantly, without any user effort or need of IT support.

This paper presents the architecture and implementation of SaaS-enabled analog design tool that breaks away from the on-premises and all automated design approach to provide design assistance that is more aligned with analog workflow. The tool is designed to give a designer a mapping and navigating console in the solution space, based on user specification, topology and target technology. Once a solution is found, a SPICE netlist of the solution is produced for the sign-off phase.

The remaining part of this paper is organized in six sections. Section II provides a brief overview of past attempts to automate analog circuits design. The overview lists approaches and computational strategies that were leveraged on in this work. Section III presents the proposed SaaS-enabled architecture as a design assistant for analog circuit design. Section IV gives an overview of the usage model for proposed analog circuit design system, Γ (Gamma). Section V provides details about algorithmic and programming aspects of implementing the proposed Γ system. Section VI presents performance results of an implementation of the Γ system, in terms of accuracy, usability and speed. Section VII gives some discussions about the proposed system and provides concluding remarks.

2. Previous work

A. Overview

After the advent of the SPICE simulator [10], academic research in the field of analog design automation has focused mainly on automating the manual design flow [11]. This was done by

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