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Statistical analysis of asynchronous pipelines in presence of process variation using formal models

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ABSTRACT

Globally Asynchronous Locally Synchronous Network on Chip (GALS NoC) is one of the possible interconnect platforms in multiprocessor systems on a chip. Designing proper links and buffers in these circuits can improve their performance. An asynchronous pipeline is a key element in buffer designs. The type of pipeline and its size can influence the performance metrics such as power consumption and delay. However, asynchronous pipelines face some challenges such as performance evaluation, verification, and process variation. We consider a new formal model to overcome these challenges simultaneously. In this paper, a new statistical model for asynchronous pipelines based on Generalized Stochastic Petri Net (GSPN) has been developed. This model can be applied to different pipeline stages, in order to compare them based on the statistical analysis of performance metrics (power consumption and delay), and to analyze their performance and timing verification in presence of variation. We have explored various kinds of asynchronous pipelines, and their corresponding results show this model has reasonable accuracy in average (below 5%) and in variance, compared to the low level Monte Carlo Hspice simulation.

1. Introduction

Today, synchronous designs face some challenges such as clock distribution and clock skew. Process variation under 45 nm technologies can reduce the reliability of digital circuits. In asynchronous circuits the elimination of global timing exhibits interesting features such as higher throughput, better EMI characteristics, and better process variation tolerance versus the synchronous counterpart.

However, asynchronous circuits encounter other challenges: performance evaluation, verification (timing and performance) and still some process variation issues. Performance evaluation of asynchronous circuits is more complicated compared to that of synchronous designs. The global clock frequency in synchronous systems is limited by the critical path. In contrast, the operation of an asynchronous circuit depends locally on the critical path of each component and globally on the average timing. Therefore, the performance evaluation in this type of circuits must be done based on the design structure, the signaling scheme between components and the environment [1]. Due to these issues the timing verification of asynchronous systems seems to be much harder. Timing assumptions and signaling between components in this type of design impose more pressure on the verification process compared to synchronous systems. Beside the correct functionality, the performance verification is another issue that must be investigated. This means that various parameters of the design (e.g. size of buffers, depth of pipelines, and structure of components) must be selected properly to satisfy performance constraints. In addition, below 45 nm technology, power consumption and transistor variation are two limiting factors of design. Due to factors such as modeling errors (inaccurate library used for device and interconnect simulations), process variation (inconsistency between parameters of simulated and fabricated device), and environment variation (unreliability caused by environment parameters like temperature or voltage) power and delay predictions are faced with unreliability. Therefore, delay variability in fabrication process can affect the functionality and performance of digital circuits [2–5]. Although asynchronous circuits show more robustness against variability in comparison with synchronous ones, the variation can still reduce performance and change functionalities of this type of circuits. Analyzing the effects of variation on different design components from performance and functionality points of view are two issues that must be examined. Presenting new models or methods for simultaneous performance evaluation and verification (timing and performance) of asynchronous circuits in presence of process variation is a research subject that must be addressed. For example, in GAELS project [6] these problems have been examined for Elastic GALS circuits.

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Different works addressing these challenges have been presented. We will examine papers related to these works. Process variation is one of the hot topics in research domain. Important sources of variation can be listed as follows [2,3]: Random dopant fluctuation (RDF), Line-edge roughness and line width roughness, Gate dielectric variation, Pattern proximity, Chemical Mechanical Polish (CMP), strain variation, Implant and anneal influence on variation.

These variation sources influence the threshold voltage as one of the main sources of variation [2,3]. This variation can affect delay, power consumption, and functionality of digital circuits. For instance, the static power is exponentially proportional to the threshold voltage; therefore, it has greater share in changing the performance of circuits compared to other sources of variations such as oxide thickness and length and width of transistors [7]. Thus, in this paper we have considered the threshold voltage variation; however our approach can also be applied to other sources of variation. Apart from these types of variation, which occur during the fabrication process, environment conditions such as temperature, activity and supply voltage variations can influence the life cycle of a circuit. These variations are called environment variation [8,9]. The process variation is categorized into two sets in terms of impact on a die. In Die-to-Die (D2D) variation, the effect of variation on a die is identical, but different from one die to another; whereas in Within-Die (WID) variation the impact on different parts of a die is different [3,10]. The timing analysis of digital circuits under variability constraints can be done using simulations with different variation conditions including best, nominal, and worst cases [5,11]. This method is called Static Timing Analysis (STA). STA is very time consuming and many samples for design performance analysis must be taken [11]. Worst case analysis in digital circuits is very complex and producing proper states for the static timing examination cannot be done within reasonable time with acceptable accuracy [11]. Therefore, deterministic methods do not offer efficient solutions for designing reliable digital circuits aware of variation problems. Due to probabilistic nature of variation sources, statistical methods have been considered [5,11]. By modeling the variation source with a probability distribution function (PDF) the designer can analyze the timing behavior of digital circuits with statistical methods. This method is called Statistical Static Timing Analysis (SSTA). SSTA benefits are listed below [11]:

- When running a mathematical algorithm the design slack time distribution can be calculated. Thereby within a shorter time the designer is capable of finding the problem of a circuit in presence of variation to improve the yield factor of chips during the design phase.
- Diagnosis of the overall performance and robustness and determination of circuits' sensitivity points in early stage of design are among the main outputs of SSTA. It not only helps designers analyze the variation effects, but also can help select proper parameters for design to improve performance parameters.

We would like to find effective methods for performance evaluation and timing analysis of digital circuits in presence of variability. Also, due to the effect of variation on the functionality of circuits [4,5], their verification in presence of variation is an attractive topic which should be considered. Developing new methods to handle simultaneously performance evaluation and verification of digital circuits under variability constraints is one of the desirable research topics [6]. As discussed above this subject in asynchronous domain is very complex compared to traditional synchronous designs. Investigating a new model for performance evaluation, verification (timing and performance), and analyzing the design in various stages can reduce the design time and subsequently time to market. Therefore, in this work we present a new high level formal model based on Petri net for different asynchronous pipelines considered as key elements in asynchronous circuits. The main features, contributions and applications of our work are listed below:

- Detailed delay modeling: in our model by using Generalized Stochastic Petri Net, each component can be modeled with its internal delays (not only input–output timing)
- Verification and performance evaluation in the same platform: with high level formal modeling and statistical analysis two goals can be achieved. Due to detailed delay modeling of pipelines verification of these circuits in presence of variation can be analyzed. In timing verification, incorrect functionality of primary pipelines in presence of variation (e.g. non synchronized data and request) can be analyzed. In performance evaluation, power and delay distributions of asynchronous pipelines with high level and fast simulation compared to the low level ones can be extracted. These distributions are helpful to evaluate performance metrics of different pipelines. Also, these distributions can be used for performance verification. In performance verification, the probability of delay and power to be in the desired interval can be estimated. This goal can be achieved through property checking in this model.
- Selecting the type of pipeline and its depth: the depth and the type of a pipeline affect its delay, power, and area. On the other hand, the process variation can move away these performance metrics form the desired points or intervals. Relying on power and delay distributions, the designer can better select depth and type of pipelines. The selected parameters for pipelines show higher probability for the performance metric to be in the desired interval. In other words, the best depth and type of pipeline taking into account the process variation can be determined.
- Sensitivity analysis: analyzing the effects of variation on special points of design and selecting better parameters on these points to overcome variation problems. In this paper the effects of threshold voltage as one of the important sources of variation have been explored. Other types of variation sources such as oxide thickness or length and width of transistors are not covered; however, our methods can be applied to these sources as well.

Note that in this paper we are only using buffer pipelines, and thus pipelines with choice are not covered and will be left as future work.

This paper is organized as follows: the related work is described in Section 2. In Section 3 preliminary concepts are defined, the model and its capabilities are explained in Section 4. The simulation results and conclusion are discussed in Sections 5 and 6, respectively.

2. Related work

In this section, the related work on the challenges explained above is discussed in the following order: performance evaluation, asynchronous pipelines, verification, and process variation.

2.1. Performance evaluation

The performance evaluation of asynchronous circuits has been explored in many other works from different angles. The first issue in performance evaluation is how the delay is modeled. Probabilistic behavior of delay in asynchronous systems [4] and random nature of process variation [12,13] lead to a statistical evaluation of performance of these systems. In [12,13] a new model based on simulation has been developed to perform SSTA on different asynchronous structures. They consider variation problem and model components with probabilistic delays of each