INTEGRATION, the VLSI journal 55 (2016) 129–137

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

A novel spatially configurable differential interface for an electronic system prototyping platform

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ARTICLE INFO

Article history:
Received 2 June 2015
Received in revised form
26 April 2016
Accepted 26 April 2016
Available online 3 May 2016

Keywords:
Reprogrammable circuit board
Wafer scale integration (WSI)
Differential signaling
Current mode logic

ABSTRACT

This paper presents complete and detailed circuit design, and the first experimental validation of a previously proposed spatially configurable differential interface that was designed to support current mode logic (CML) on a reconfigurable electronic system prototyping platform. The physical and electrical constraints of CML interfaces are described, and an architecture is proposed for transmitting differential signals between two different integrated circuits (ICs) deposited on the prototyping platform surface. The proposed implementation has been validated in a test-chip using a mature 0.18 μm CMOS technology. Measurements on the test-chip show that the spatially configurable differential interface can operate at a speed of up to 2.5 Gbps.

Contents

1. Introduction

In today's high-end electronic systems, higher complexity integrated circuits are being put together to provide as much performance and features as possible in one single product. This complexity is posing many challenges in different stages of product development, which are exacerbated by the short time-to-market imposed on the developers due to the competitive nature of the industry.

Simulation platforms and design flows that are used to validate integrated circuits during their development stages are quite mature. Hardware emulation platforms, such as the ones based on FPGAs [1–3] and ASICs [4,5] can support very complex integrated circuits. Nevertheless, there is no commercially available automated prototyping and testing platform for electronic systems

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http://dx.doi.org/10.1016/j.vlsi.2016.04.008
0167-9260/

built with integrated circuit (IC) components like microprocessors, ASICs, memories and FPGAs. Printed circuit boards (PCB) are still essentially the only technology for prototyping such systems, but design and manufacturing of complex PCBs can take from several weeks to months. Most of the electronic systems require software in addition to the hardware itself. The sooner a working hardware prototype can be provided for the software team to work on, the faster the overall product development can proceed.

Current trends for technologically and economically viable reconfigurable system solutions include a variable combination of FPGAs and other kinds of programmable logic, application-specific instruction set processors (ASIPs), and systems implemented with coarse-grained reconfigurable hardware (different from ASIPs) [6]. An active reconfigurable board, called the WaferBoard, has been proposed in [7]. The reconfigurable board is intended to be a multi-purpose prototyping platform, which provides programmable interconnections among multiple user ICs (uICs) like ASICs, memories and FPGAs. The WaferBoard, intended as an alternative to PCBs, is designed to support as many types of ICs and signal interfaces as possible. One such signal interface is differential signalling, widely used in high speed data transmission. Standards, currently in use for differential signalling, include for instance LVDS (low voltage differential signalling), LVPECL (low voltage positive emitter-coupled logic), CML (current mode logic), and HSTL (high-speed transceiver logic) [8]. The example in Fig. 1(a) shows a basic MOS CML buffer. It includes two pull-up resistors R_D, two nMOS transistors for switching and a current source I_{TAIL}. The voltage swing is generated by switching the current in a common-source differential pair. Since the nMOS transistors are always saturated and there are no pMOS transistors, inputs and outputs based on these circuits can operate at more than 3 Gbps, which is faster than the typical maximum speed of CMOS logic implemented with devices of comparable size driving similar loads [9]. Solutions to propagate differential signals on a wafer or for inter-die communication has been proposed in [10–12]. Unfortunately such approaches do not offer spatial reconfiguration and thus are incompatible with reconfigurable systems such as the WaferBoard or FPGAs.

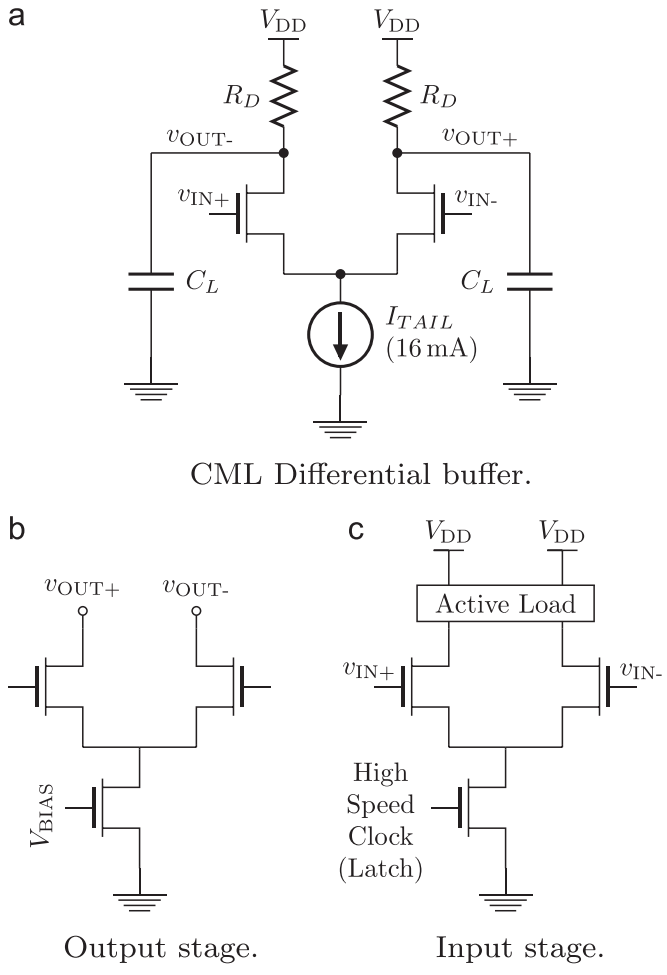

Fig. 1. CML structure.

This paper presents a complete and detailed circuit design and the first experimental validation of a spatially configurable CML interface originally introduced but not experimentally validated in [13,14]. The circuit design was implemented using a standard CMOS process that is fully compatible with the WaferBoard platform and which could be adapted and used in any integrated circuit with programmable I/Os such as FPGAs. Besides the research conducted by our team, that concept remains unexplored in the literature. The focus of our research was not to support only CML, but in addition to supporting conventional CMOS I/Os, to develop a means to support spatially configurable propagation paths for differential-to-single-ended conversion that can be later enhanced to accommodate other differential signaling standards in the WaferBoard or in integrated circuits with programmable I/Os. We chose CML as a representative differential signaling technique for the prototype test-chip that was designed, fabricated and tested and for which conclusive experimental results are reported for the first time in this paper. CML was chosen because of its popularity and simplicity. A prototype test-chip, that was fabricated and tested, demonstrates the feasibility of the proposed interface that could support differential signalling in the prototyping platform. Section 2 describes the specifications for compatibility with the WaferBoard, as well as the electrical and physical constraints imposed by differential interfaces. Section 3 describes the differential interface architecture and its complete and detailed circuit design. Section 4 reports measured results from the test-chip implemented using a 0.18 μm CMOS technology. Finally, we conclude in Section 5 by summarizing our main results.

2. Background

2.1. Compatibility with waferboard, a prototyping platform for electronic systems

The core of the WaferBoard platform upon which uICs are to be deposited is called the WaferIC™. Its surface has a dense array of very fine (tens of microns) conducting pads, called NanoPads. Each NanoPad is connected to an internal wafer-scale interconnect network, called WaferNet™, that can be configured to connect a NanoPad to any other NanoPad, without any conflicts among large sets of connections. Whatever the position and location of the uICs are on the WaferIC, the NanoPads are able to make contact with their solder ball pins. So hand placement of uIC is sufficient, as shown in Fig. 2(a) and (b). When a uIC pin (solder ball) makes contact with several NanoPads, the WaferIC detects and maps contacted pins, and the WaferNet is then automatically configured according to connected NanoPads and the user netlist [7]. Subsequently, a reconfigurable signal propagation channel is established according to the users requirement, as shown in Fig. 2(c). PCBs can provide the same connections but in a way that is not configurable. As a result, PCBs need to be redesigned if any change is made in the electronic system. Even though PCBs can provide "hard-wired" optimized high-speed connections for a particular application, WaferBoard can provide re-configurable connections that typically function at a lower speed.