Microelectronic Engineering 119 (2014) 1–5

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Design and fabrication of a multiple-thickness electrochemical cantilever sensor

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ARTICLE INFO

Article history:
Available online 23 January 2014

Keywords:
Fabrication
Cantilever sensor
Thickness
Electrochemical

ABSTRACT

This paper presents a new design and fabrication process of a multiple-thickness electrochemical cantilever sensor, in order to assess the role of the cantilever's thickness on the chemically-induced mechanical effects. Each cantilever can act not only as a functionalized cantilever, but also as an independent working electrode (WE) for electrochemical measurement. The different thicknesses of the silicon nitride layer are achieved by successive masking and reactive ion etching of partially overlapping openings at a low etch rate (10.8 nm/min, 15.8 nm/min, 20.1 nm/min, or 26.5 nm/min). A small-scale thickness difference (<30 nm) is successfully obtained. One advantage of this fabrication process is that the thickness distribution of cantilevers can be altered and broadened by combination of different RIE recipes or modification of the etching time. In addition, the integration of the cantilever chip with a fluidic cell, a printed circuit board (PCB) and a temperature-controlled plate to form a hybrid system is also addressed.

1. Introduction

In the last decades, the ability of cantilever sensors to detect a wide range of molecular interactions has been demonstrated [1]. Cantilever sensors are usually operated in either dynamic or static mode [2]. In dynamic mode, absorption or adsorption of analyte molecules leads to a shift of the resonance frequency. In static mode, the cantilever bends as a result of preferential adsorption of analyte molecules on one side of the cantilever. The dynamic mode is sensitive to mass variations whereas the static mode is sensitive to surface effects.

For cantilever sensors in the static mode, the cantilever's curvature change is assumed to be homogeneous [3] and is used as an indicator that the thought reaction occurred. In order to increase the sensor's specificity, various groups have focused on improving the performance of cantilever-based sensing by introducing an electrochemical actuation [4–7]. However, it is questionable to interpret the cantilever deformation through Stoney's equation when dealing with chemically-induced effects. To address this issue, alternative mechanical frameworks have been proposed [8,9], featuring different relationships between the cantilever's thickness and the shape of the displacement field. These models differ by the way the thickness of the cantilever is involved. Therefore, testing for the validity range of these models requires to experimentally access chemically-induced displacement fields [8,9] obtained for cantilevers of different thicknesses. In order to achieve that with cantilevers featuring the same material properties, our goal is to fabricate multiple-thickness cantilever beams in a single chip. The values of material parameters driving the dependence on thickness however remain unknown, and the achievable thickness distribution in turn define the range of accessible material parameters. This first attempt is thus intended to explore the achievable thickness range. The fabricated chip is to be placed in a fluidic cell in order to monitor the cantilevers' displacement field when they are subjected to a surface (electro-) chemical modification.

It is extremely challenging to achieve micro-fabrication of multiple-thickness cantilever beams on a single chip, simultaneously ensuring their combined electrochemical and mechanical capabilities as well as the necessary accessibility for optical readout, electrical connection, and fluid access for real-time deflection measurements. In this work, we focus on the design and fabrication of a multiple-thickness cantilever sensor platform. In addition, the assembly of the hybrid system featuring the obtained cantilever chip, a fluidic cell, a homemade printed circuit board (PCB), and a temperature-controlled plate is also presented.

2. Materials and methods

2.1. Configuration of the hybrid system

The proposed hybrid system is depicted in Fig. 1, integrating a fluidic cell, the cantilever chip, a printed circuit board (PCB), and

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http://dx.doi.org/10.1016/j.mee.2014.01.009

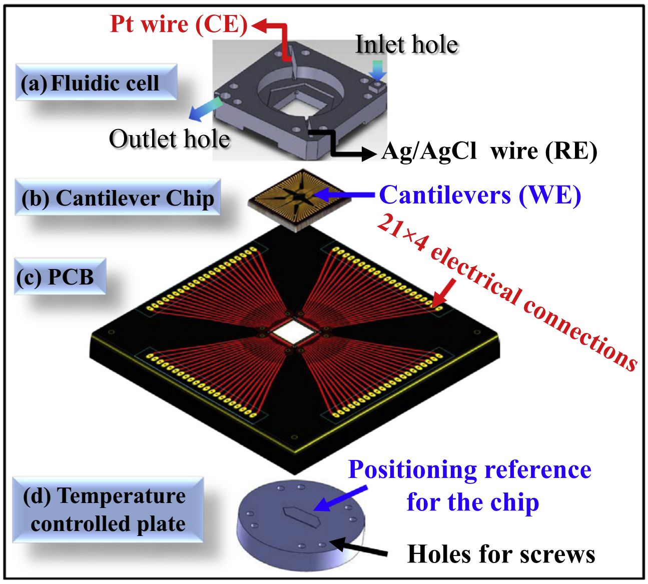

Fig. 1. Configuration of the deflection measurement hybrid system: (a) fluidic cell, (b) cantilever chip, (c) printed circuit board (PCB), and (d) temperature-controlled plate.

a temperature-controlled plate. The fluidic cell is designed to hold liquid and to set an electrochemical cell. It provides fluidic inlet and outlet, and includes two channels for inserting a reference electrode (RE) and a counter electrode (CE). The cantilever chip includes four identical cantilever arrays. Each cantilever array houses 20 cantilever beams featuring different thicknesses. Each cantilever is used as the independent working electrode (WE) and also as the functionalized platform. In order to contact the cantilevers, a home-made PCB is designed to electrically connect the cantilever chip by wire bonding. A small square hole (12.8 mm × 12.8 mm) in the middle of the PCB allows the backside of the cantilever chip to directly contact with a temperature-controlled plate. The positioning reference is used to achieve a reproducible positioning of the chip with respect to the temperature-controlled plate.

4 Rods through the corresponding holes provide an alignment reference when the fluidic cell is bonded to the front side of the cantilever chip (which is firstly glued on the PCB). The entire assembly is pressed together via 4 screws through the other 4 holes and 4 spring clips mounted on the temperature-controlled plate.

2.2. Fluidic cell

The fluidic cell is designed by using the SolidWorks 2011 software and fabricated by a 3D printer (3D Systems ProJet™ SD 3500). The obtained poly (methyl methacrylate) (PMMA) fluidic cell is shown in Fig. 1. It is 3.8 mm thick, 22 mm wide, and 22 mm long. A 0.5 mm-thick hexagon step of the cavity is designed to glue a Pyrex slice (10 mm diameter, 0.17 mm thick, not shown in Fig. 1). The whole fluidic chamber volume is 37 µL with the cover glass. 8 holes are used to insert 4 rods for positioning the fluidic cell with respect to the front side of the cantilever chip, and 4 screws for fixing the full assembly.

2.3. Cantilever chip

The proposed chip features: (a) a positioning reference on the backside, (b) multiple cantilever thickness on the front side, (c) an electrode layer, (d) an electrical connection layer, and (e) an insulation layer. In the following, the fabrication process is described by using two cross sections and by focusing on cantilever No. 9, shown in Fig. 2.

(1) In Fig. 2b, low-stress silicon nitride is first deposited on both sides of a four-inch silicon (1 0 0) wafer with 500 µm thick by Low Pressure Chemical Vapor Deposition (LPCVD) (NH_3/SiH_2Cl_2: 18/60 sccm, temperature: 820 °C, pressure: 200 mTorr, time: 180 min). The silicon nitride thickness is measured to be about 805 nm. After baking the wafer for 10 min at 120 °C, the wafer is spin-coated with a 2.4 µm thick layer of SPR 220-3.0 positive photoresist. Then, the photoresist is exposed to UV irradiation (365 nm, 300 mJ cm^{-2}) through a mask with the designed alignment reference pattern. After developing the photoresist with the MF 26A developer for 75 s, the exposed silicon nitride is reactive ion etched at a 26 nm/min etch rate (pressure: 60 µbar, CHF_3/C_2F_6: 10/5 sccm, DC bias: 245 V; RIE PLASSYS). Afterwards, the photoresist is stripped.

(2) The cantilever beams (15 µm wide and 80 µm long) are patterned on the front side of the wafer by using double-side EVG 620 alignment system. Then, the pattern of cantilever beams is achieved by reactive ion etching (RIE) of the exposed silicon nitride layer (shown in Fig. 2c). The whole RIE time (40 min) is divided into two 20 min etching times, with 30 s oxygen surface cleaning process (20 sccm, 60 µbar, 95 W, 410 V) in between. Then, the photoresist is stripped.

(3) To achieve different cantilever thicknesses, a single mask is specially designed and successively used with different alignment marks. Using this mask referring to mark 1 (shown in Fig. 2d), some of the cantilever beams are firstly covered by photoresist (SPR 220-3.0, 2.4 µm thick). The photoresist pattern is used as an etching mask in the RIE etching process with a low etch rate (10.8 nm/min, 15.8 nm/min, 20.1 nm/min, or 26.5 nm/min) for 1 min. Shifting the mask by referring to mark 2 (shown in Fig. 2e), partially overlapping openings are photo-patterned and etched by another 1 min RIE. In Fig. 2f, this step is repeated twice by shifting the mask referring to mark 3 and mark 4, respectively. By successive photo-patterning and etching of partially overlapping openings, different thicknesses are thus achieved.

(4) Corresponding to Fig. 2g, a Cr/Au (10 nm/30 nm) electrode layer is deposited by electron beam evaporation (EVA 450, Alliance Concept), and then lift-off in selected areas by dissolving the underlying photoresist. In order to independently bridge the electrode layer to electrode pads on borders of the chip, one electrical connection layer is added. This connection layer (Cr/Au: 20 nm/250 nm) is sputtered (MP 500, PLASSYS) and shaped by lift-off process. A potassium hydroxide (KOH) solution (28%, 1 h at 80 °C) is used to etch 60 µm of silicon on both sides of the wafer, thus releasing the cantilevers and defining the alignment reference. Finally, the electrical connections are insulated by spray coating (AltaSpray 8) a 7 µm thick SU-8 layer.

3. Experimental results

3.1. The repeatability and stability of RIE

The repeatability and stability of RIE is critical to obtain a well-defined thickness difference. By using RIE PLASSYS machine, we have developed four recipes (shown in Table 1). Keeping the same pressure and the same gas flow rates, we can obtain four different etch rates by changing the DC bias voltage. As shown in this table, recipe No. 2 has the best stability with a 0.68 nm/min standard deviation.