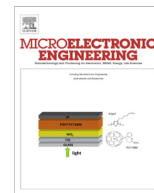
Microelectronic Engineering 119 (2014) 95–99

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee



Buried triple-gate structures for advanced field-effect transistor devices

M.R. Müller [a,e,*], A. Gumprich [a], F. Schütte [a], K. Kallis [a], U. Künzelmann [b], S. Engels [c,d], C. Stampfer [c,d], N. Wilck [e], J. Knoch [e,*]

[a] *Intelligent Microsystems Chair, TU Dortmund, Emil-Figge-Str. 68, 44227 Dortmund, Germany*
[b] *Institute of Semiconductor and Microsystems Technology, TU Dresden, 01062 Dresden, Germany*
[c] *JARA-FIT and 2nd Institute of Physics, RWTH Aachen University, 52074 Aachen, Germany*
[d] *Peter Grünberg Institute (PGI-9), Forschungszentrum Jülich, 52425 Jülich, Germany*
[e] *Institute of Semiconductor Electronics, RWTH Aachen University, Sommerfeldstr. 24, 52074 Aachen, Germany*

A R T I C L E   I N F O

Article history:
Received 14 November 2013
Received in revised form 26 January 2014
Accepted 2 February 2014
Available online 6 March 2014

Keywords:
Electrostatic doping
Buried triple-gate structure
Band-to-band tunneling
Graphene nanoribbon FET

A B S T R A C T

One key element in the investigation of novel channel materials and device principles is the realization of an appropriate source–drain doping profile. The paper at hand describes the manufacturing of a buried triple-gate (BTG) structure, where three separately addressable gates are implemented to control the charge carrier density within source, drain, and the channel of a field-effect transistor. The BTG structure is optimized for the investigation of graphene, and a 30 nm graphene nanoribbon is fabricated on top of the structure. Electrical measurements at 25 K indicate the successful realization of p-n junctions and demonstrate band-to-band tunneling at the source–channel and channel–drain interfaces.

© 2014 Elsevier B.V. All rights reserved.

1. Introduction

Improvements of the performance of integrated circuits have traditionally been achieved by scaling down the dimensions of MOSFET devices. However, the appearance of short-channel effects requires the use of ultrathin channel layers in order to preserve electrostatic integrity of the scaled transistors (see e.g., Skotnicki et al. [1] and references therein). Furthermore, novel channel materials with a higher carrier mobility than silicon are intensively investigated, since they enable a further performance benefit without scaling. As a result, the 2011 ITRS roadmap states that, "in the long term", in order, "to attain adequate drive current for the highly scaled MOSFETs, high transport channel materials such as", [...], "semiconductor nanowires, carbon nanotubes, graphene or others may be needed" [2]. In addition, novel device principles, such as the Tunnel FET (TFET), become more interesting especially for low power applications [3–10].

However, a major challenge for the investigation of novel channel materials is the realization of an appropriate source–channel–drain doping profile, because conventional (e.g., impurity, chemical) doping is often not possible, extremely challenging [11–13], or, in the case of TFETs, the right amount of doping is subject to tedious optimization [14,15]. A viable alternative is source–drain doping by means of electrostatic potentials; this approach not only allows easy, but moreover adaptable source–drain doping during electrical measurements. Electrostatic doping has already been employed to investigate carbon nanotube, graphene, and nanowire TFETs [3,13,16–19]. However, devices based upon electrostatic doping so far either use only two gates or employ chemical doping that does not allow manipulating the carrier density over a wide range. Here, we describe the development and manufacturing of a buried triple-gate (BTG) structure with three individually controllable gates serving as a platform for the investigation of various nanoobjects. More specifically, the three gates can be used to realize nFETs (pFETs), i.e., an n-n (p-p)[1] doping profile, or TFETs with an n-p[2] doping profile. Since the electrostatic environment is determined by the BTG structures irrelevant of the nanoobject under investigation, our BTG structures allow for a true comparison of various materials in terms of their suitability for future FET devices. Exemplary, the BTG structure is used to successfully realize n-p doping for a 30 nm graphene nanoribbon FET.

* Corresponding authors. Address: Intelligent Microsystems Chair, TU Dortmund, Emil-Figge-Str. 68, 44227 Dortmund, Germany. Tel.: +49 231 755 4301; fax: +49 231 755 4450 (M.R. Müller). Tel.: +49 241 802 7890; fax: +49 241 802 2246 (J. Knoch).

E-mail addresses: marcelrene.mueller@tu-dortmund.de (M.R. Müller), knoch@iht.rwth-aachen.de (J. Knoch).

[1] n-n (p-p) means n- (p-)doped source and drain side-gate regions.
[2] n-p means n-doped source side-gate and p-doped drain side-gate regions.

http://dx.doi.org/10.1016/j.mee.2014.02.001
0167-9317/© 2014 Elsevier B.V. All rights reserved.

2. Buried triple-gate structure

The BTG structure consists of an aluminum center gate surrounded by n-doped Si side-gates for the purpose of electrostatic doping. The electrical isolation is obtained by silicon dioxide enclosing the n-Si, and a thin Al_2O_3 dielectric on top of the aluminum. The floor plan in Fig. 1(a) shows that a closed meander of the aluminum gate (purple) yields two isolated n-Si regions. The inner region (cyan) is used as source side-gate and the outer region (orange) as drain side-gate. The meanders cover approx. 80% of the sample surface, i.e., nanoobjects deposited randomly on top are likely to lie across the aluminum center gate reaching over the side-gates. In Fig. 1(a), a graphene nanoribbon (GNR) is exemplarily shown. After the deposition of the nanoobjects, source–drain contacting over the side-gate regions completes, e.g., a nanowire device. For graphene, nanoribbons have to be manufactured additionally. Note that the electrostatic environment that determines the electronic properties of an FET is the same no matter which nanoobject is investigated.

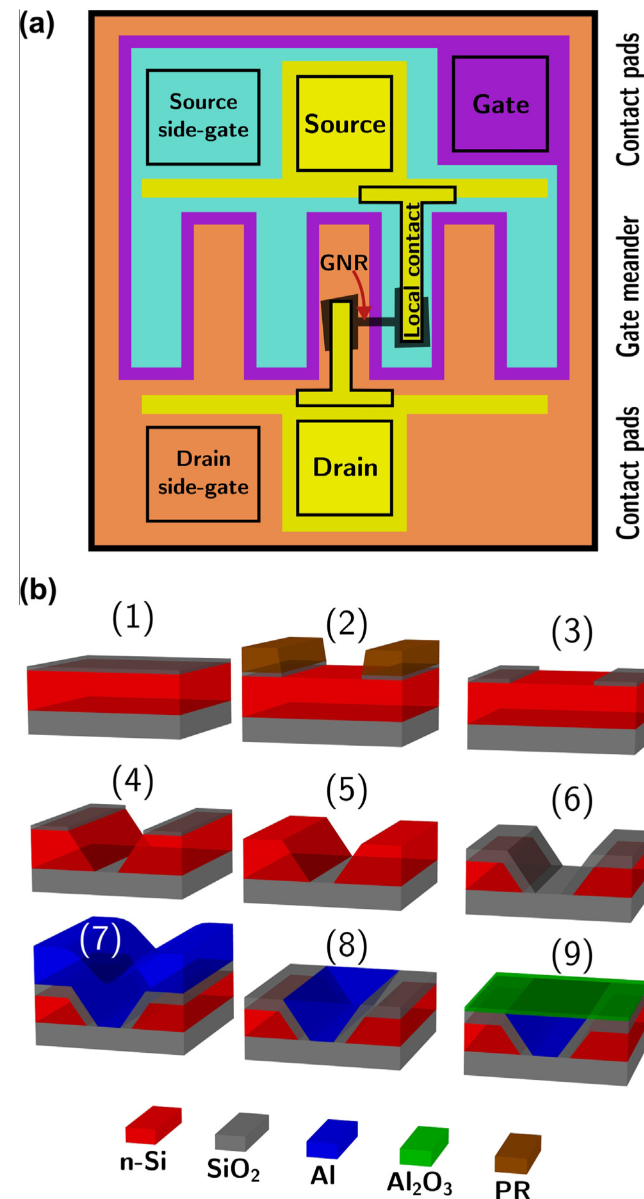


Fig. 1. Floor plan (a) and manufacturing process (b) of the BTG structure.

The BTG structures are arranged in isolated and identical fields of 0.5 × 1 mm, each gate meander has a length of approx. 24 mm; the width of the aluminum meander, i.e., the gate length, is either 0.6, 1 or 2 μm, which allows a processing sequence solely based on optical lithography. Note, that the fabrication scheme is suitable for a combination of optical and electron-beam lithography enabling a further downscaling of the gate length. However, we are mostly interested in studying nanoobjects in a TFET configuration, and it was shown that the performance of TFETs is, to a large extent, independent of the channel length [9]. Thus, different gate (i.e., channel) lengths were only realized to enable the investigation of nanoobjects of different geometrical size.

Fig. 1(b) illustrates the manufacturing process of the BTG structure. The starting material is a 4-inch SOI-wafer with a top-layer of 340 nm (100)Si and a 400 nm buried oxide (BOX). The silicon is implanted with $1 \cdot 10^{15}$ cm^{-2} of phosphorous at 75 keV, 7.5°, yielding a peak implantation depth of 104 nm. Afterwards, the wafer is RCA-cleaned, and a 20 nm layer of SiO_2 is grown using dry thermal oxidation thereby healing implantation damage and activating the dopants (1). Optical lithography is used to pattern the oxide layer using buffered oxide etch (BOE) (2). After removal of the photoresist (3) and directly after an additional BOE dip, tetramethylammonium hydroxide (TMAH), 25 wt.% at 80 °C is used to anisotropically etch through the SOI layer [20] (4). The oxide mask is removed using BOE (5), and the side-gates are electrically insulated by wet thermal oxidation (6). Subsequently, aluminum is sputter-deposited onto the surface (7), and chemical–mechanical planarization (CMP) is employed to remove the Al overburden yielding an entirely planar structure (8). The slurry in use (NOVUS™ A7100 A/B by Cabot Microelectronics) was found to produce smooth interfaces, exhibit extremely high Al/SiO_2 selectivity and low dishing (see below) [21]. The gate dielectric on top of the aluminum center gate was obtained by atomic layer deposition (ALD) of Al_2O_3 (9). The BTG structures were completed by selectively etching the oxides using CHF_3 + Ar plasma in the contact regions and a subsequent deposition of 180 nm Ti + Au contact metal using a lift-off technique. The finished wafer was cut into sample pieces of 7.5 × 7.5 mm^2.

Scanning electron microscopy (SEM) cross-section images of the BTG structure reveal a side-gate oxide thickness of 95 nm (cf. Fig. 4), the Al_2O_3 (not visible) thickness is approx. 7 nm. Atomic force microscopy (AFM) surface scans of the same sample (not shown) indicate that the polished aluminum exhibits excellent planarity with a dishing of 4.1 nm for an Al-structure width of 1.3 μm and low roughness (down to 1 nm root mean square) [21]. Note that the dish-shaped, darker section of the Al gate in the cross-section of Fig. 4 is not the dishing of the surface, but due to the non-ideal breaking edge after cleavage of the sample.

3. Visibility of graphene on buried triple-gate structures

Graphene has recently attracted an increasing attention; since being a monolayer of carbon it represents an ultrathin channel layer thus allowing superior gate control, and due to its excellent electronic transport properties it is promising for the realization of future high performance FET devices.

Since exfoliated graphene is still superior in terms of defect density etc., an important point of consideration when designing the BTG structures was the visibility of a monolayer graphene. While it is well known that graphene is fairly well visible on a 90 nm SiO_2/Si stack [22], the BTG stack (Al_2O_3/SiO_2/Si/SiO_2/Si) has different optical properties that depend on the thicknesses of the various layers. We therefore implemented a computer simulation for the visibility of graphene on the BTG stack in order to find the optimum thickness of the SiO_2 layer in the side-gate regions

Download English Version:

https://daneshyari.com/en/article/542606

Download Persian Version:

https://daneshyari.com/article/542606

Daneshyari.com