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Reliability study of power RF LDMOS device under thermal stress

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Abstract

This paper presents the results of comparative reliability study of two accelerated ageing tests for thermal stress applied to power RF LDMOS: Thermal Shock Tests (TST, air–air test) and Thermal Cycling Tests (TCT, air–air test) under various conditions (with and without DC bias, TST cold and hot, different extremes temperatures ΔT). The investigation findings of electrical parameter degradations after various ageing tests are discussed. On-state resistance (R_{ds_on}) is reduced by 12% and feedback capacitance (C_{rss}) by 24%. This means that the tracking of these parameters enables to consider the hot carrier injection as dominant degradation phenomenon. To reach a better understanding of the physical mechanisms of parameter's shift after thermal stress, a numerical device model (2D, Silvaco-Atlas) was used to confirm degradation phenomena.

Keywords: Simulation; Hot carrier effects; LDMOS; Thermal stress

1. Introduction

RF LDMOS is becoming increasingly important in communication sector, such as mobiles, portable computers and eventually base stations, thus generating ongoing effort demand to improve performances. The device's lifetime is one of the criteria used to qualify a technology. Temperature is a critical parameter, particularly in RF power electronic devices. This element has a considerable influence on reliability and performances [1,2], can limit the lifetime of semiconductors and consequently plays an essential part in failure mechanisms [1,3]. For these reasons thermal shocks and cycling conditions are becoming important for RF LDMOS in many applications. It is well-known that if devices are repeatedly subjected to electrical and thermal overload over extended periods of time, shock and cycling phenomena may lead to device failure, leaving the load current unlimited and therefore leading to serious risk of damage [4]. The objective of the presented work is a comparative reliability study of various thermal stress conditions, respecting to other studies in the literature. The methodology consists in characterizing and modelling the device before and after ageing.

2. Device experimental characterization and parameters extraction

It is essential to characterize power RF LDMOS in order to extract parameters before and after device stress. This step would enable us to correlate thermal stress to any parameter drift, or even to help identify a degradation phenomenon. A commercial Motorola RF LDMOS has been used for this study. The main characteristics of this device can be listed as follows: frequencies up to 2 GHz, output power of 10 W, breakdown voltage of 65 V. I–V and C–V measurements were performed using the commercial software package IC-CAP.

The static mode I–V gives us an insight into the device behaviour in its various operating modes (linear, saturated, etc.), and allows to quantify some important electrical parameters before and after device stress. These measurements were performed by an Agilent E5270 DC analyser with 20 W power supply. The device was mounted on a Peltier module in order to stabilize the self-heating during DC measurements. The use of data management under IC-CAP allows checking the consistency of measurements [5].

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From these measurements, on-state resistance (R_{ds_on}) was deduced as a critical electrical parameter.

C–V profiles were performed using an HP 4194A impedance analyser, with a 2-pin method (which yields the total capacitance between the measurement pins: C_{rss}), the third transistor pin being unconnected [5]. These electrical parameters (R_{ds_on}, C_{rss}) will be helpful in our reliability study to keep track of electric device degradation state. In this study, for each test conditions, five samples have been tested to ensure the reproducibility of the results.

To quantify the parameter shift that appears after ageing, a new electro-thermal model was used for power RF LDMOS devices as a reliability tool [6]. It has been implemented in Agilent's ADS software using Symbolic Defined Device (SDD), by providing a more accurate and flexible model. For simplicity, the new IC-CAP plot optimizer feature was applied instead of direct model parameter extraction.

The qualitative understanding of physical phenomenon is also presented. A modified 2D RF power N^- channel LDMOS structure previously developed by Raman et al. [7] was implemented and simulated using the physical simulator Atlas of Silvaco [8]. Fig. 1 shows the device's structure with approximate doping wells. The main geometrical and technological parameters are given in Table 1. The implemented structure is typically similar to our tested device. The suggested structure has a Gaussian doping profile along LDD and channel surface. The doping profile was optimized using a 2D technological process simulation carried out by SSUPREM3 [8], see Fig. 1.

3. Thermal stress bench

In our experiments, the devices are stressed with an applied drain–source voltage (V_{ds}) of 40 V and a gate–-source voltage (V_{gs}) of a value to obtain a permanent drain–source current (I_{ds}) less than 10 mA (without a self-heating effect), that corresponds to the quiescent current at ambient temperature. The thermal stresses were performed with a THERMONICS T-2820 Precision Temperature Forcing System (PTFS). The system is most commonly used for direct testing of semiconductor components at temperature extremes while they are on an auto-tester performance board. This enables measurement of all

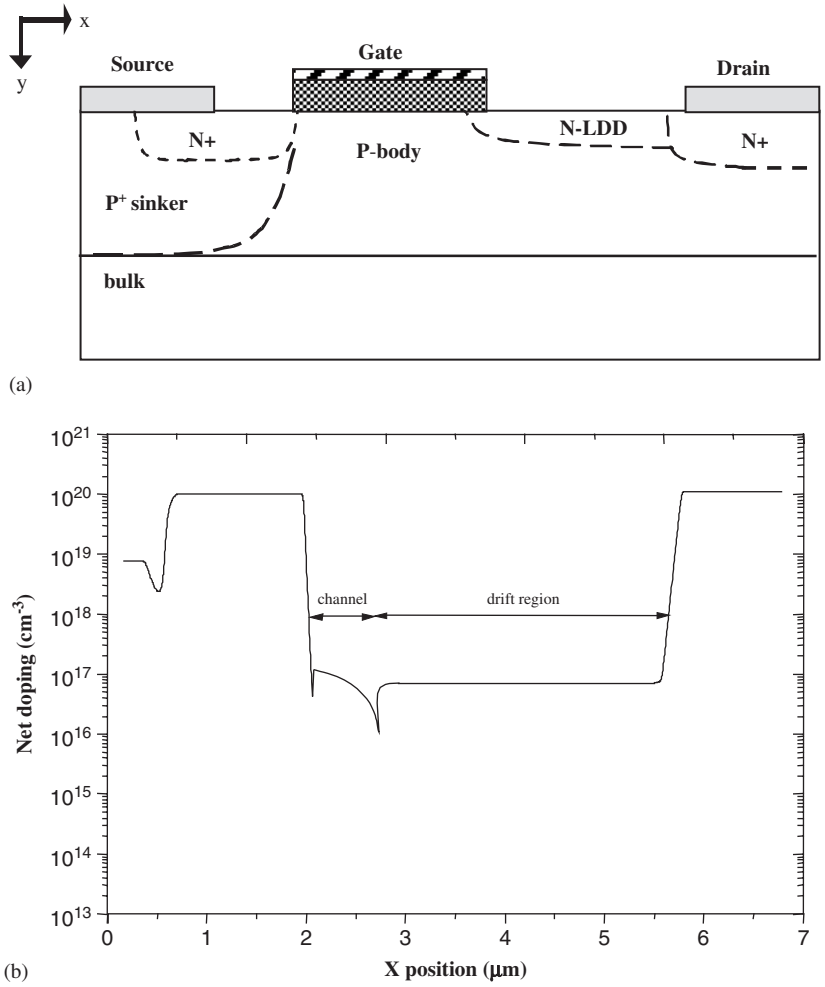

Fig. 1. (a) Cross-section view of RF LDMOS device implemented in Silvaco-Atlas, with its intrinsic capacitances and (b) Net doping profile along silicon surface.