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Impact of technology scaling on the tuning range and phase noise of mm-wave CMOS LC-VCOs ☆

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ABSTRACT

The impact of CMOS technology scaling, on the tuning range and phase noise performance of mm-wave LC voltage controlled oscillators (LC-VCOs) is presented. As a preliminary step, the fundamental LC-VCO elements (i) tank inductor, (ii) fixed and variable capacitor elements, and (iii) cross-coupled transistor pair are analytically modeled across the frequency range 10–50 GHz. These models are then exploited to analyze the tuning range and phase noise revealing the ultimate performance bounds for simultaneously achieving low phase noise and wide tuning range in mm-wave CMOS LC-VCOs across the CMOS technology scaling (from 130 nm down to 45 nm) are explored. The analysis demonstrates the improvement of the maximum achievable tuning range, phase noise, and figures-of-merit (*FoM* and FoM_T) with the technology down scaling. Finally, the performance trend of the mm-wave CMOS LC-VCOs implemented using both thin and thick gate cross-coupled pair is compared. The analysis indicates that thick gate cross-coupled pair VCOs achieve better phase noise at the expense of power consumption and maximum tuning range.

1. Introduction

The drastic increase in commercial mm-wave applications necessitates low-cost, wide tuning range (*TR*) and low phase noise VCOs. These applications include 5th generation mobile networks (5G), gigabit wireless (WiGig), 77 GHz automotive short range radar, 94 GHz passive imaging, Local Multipoint Distribution System (LMDS), satellite commercial data, and video links [1–7]. The low cost, low power consumption, high yield and high integration levels of CMOS technology have positioned CMOS VCOs for mainstream high-volume mm-wave applications.

The mm-wave CMOS VCOs are expected to benefit from the sustained scaling of device finger length, gate oxide thickness and parasitics reduction which leads to higher f_T and f_{max} [8–13]. This implies high transconductance (g_m) that can be extended to the mm-wave space with much smaller device footprint, resulting in lower device capacitance. Nevertheless, there are adverse aspects of scaling such as the increase of flicker noise and the supply decreasing headroom.

Across all CMOS technologies, there are fundamental challenges that still remain as major limiting factors in the mm-wave VCO performance [14–19]. Foremost, the quality factor (Q) of the capacitive tuning elements is sharply degrading with frequency, and hence becomes the predominant factor in the overall tank Q. This requires the use of large transistors to provide sufficient g_m, which increases the transistor capacitive loading on the LC-tank resulting in a sharp reduction of *TR*.

In most CMOS technologies, thin gate and thick gate transistors are integrated in the same technology to provide solutions for low and high voltage applications simultaneously. Thick gate devices allow the use of high supply voltages which translates to low thermal phase noise in the VCO domain. However, this phase noise improvement comes at the expense of low operating frequency, reduced *TR*, and increased power consumption. Albeit, thick gate devices have larger footprint compared to thin gate devices which results in reduced flicker phase noise.

Several techniques have been proposed to extend the *TR* of mm-wave VCOs [20–28]. However, it is very crucial to have a solid understanding of the key limitations imposed by the scaling of CMOS technology on the realization of mm-wave LC-VCOs. This paper utilizes an analytical *TR* and phase noise model to predict the VCO performance trends across scaled CMOS technologies, covering 130 nm, 90 nm, 65 nm and 45 nm processes and establishing several performance bounds. The *TR* is analyzed by decoupling the interdependence of the LC-tank elements and the cross-coupled pair. The paper is organized as follows: Section 2 studies the key limitations imposed by the LC-tank elements and the negative g_m

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cross-coupled transistors across different CMOS technology nodes and mm-wave frequencies. A detailed *TR* analysis along with minimum phase noise and figures of merit (*FoM* and FoM_T) bounds are presented in Section 3. Then, Section 4 provides a comparison between VCOs implemented using both thin gate and thick gate cross-coupled devices. Finally, the paper is concluded in Section 5.

2. LC-VCO design

LC-VCOs consist of a resonant LC-tank and a negative g_m stage that provides gain to compensate for the losses of the LC-tank. In this paper, a top-biased cross-coupled NMOS LC-VCO[1], shown in Fig. 1, is utilized due to its superior phase noise performance [29]. The following subsections independently analyze the LC-tank elements and the cross-coupled transistor pair across the frequency range 10–50 GHz for the CMOS technology nodes ranging from 130 nm down to 45 nm. The objective is to study the key limitations and performance trends of the LC-VCOs across the different CMOS technology processes in the frequency range of interest. A list of LC-VCO parameters[2] is given in Table 1.

2.1. LC-Tank

2.1.1. Inductor

A differential center-tapped spiral inductor, shown in Fig. 1, is utilized in this analysis for higher *Q*-factor and smaller die area [30]. Due to the lack of accurate foundry models for inductors at mm-wave frequencies, Sonnet EM is used to capture the inductor behavior. It is worth noting that the range of inductance used throughout this analysis varies depending on the operating frequency, as discussed in [19]. Hence, an accurate model is needed to cover the inductance range from 50 pH to 400 pH across the frequency range 10–50 GHz. Therefore, the Sonnet *S*-parameter model is simplified to a high order polynomial equation that can vary the outer dimension (d_L) for a given spiral width (W_L) to predict the equivalent inductance (L) and parallel resistance ($R_{p,L}$) across frequency, as illustrated in [19].

In order to demonstrate the validity of the model, the EM simulated and fitted L, $R_{p,L}$ and quality factor (Q_L) are plotted in Fig. 2 for the 130 nm technology node at a W_L of 8.5 μm. The model accurately capture L and $R_{p,L}$ across frequency, and hence can replace the Sonnet *S*-parameter model.

As the technology scales down, more metal layers are added but the stack height decreases leading to the implementation of the inductor on thinner metal layers that are closer to the substrate, shown in Fig. 3(a). This results in the degradation of $R_{p,L}$ at finer process nodes and as the frequency increases, which can be observed in Fig. 3(b).

2.1.2. Coarse tuning capacitors

The frequency fine tuning of the LC-VCO is realized using accumulation MOS varactors (A-MOS), shown in Fig. 1, due to its wide *TR* [31]. Coarse tuning is employed to minimize the VCO gain, and hence minimize the phase noise through AM–PM noise conversion [32,33]. The coarse tuning structure is realized using either digitally switched capacitors [34], depicted in Fig. 4(a), or digitally switched varactors [36], depicted in Fig. 4(b).

The switched varactors have the advantage of turning the capacitance ON and OFF inherently by switching between accumulation/depletion regions of operation without using a switch [35]. Since scaling the size of the varactor to increase its capacitance automatically results in lowering its effective series resistance, the varactor has a relatively fixed capacitance tuning ratio (m) which is decoupled from its losses, where

$$m = \frac{C_{V/on}}{C_{V/off}} \tag{1}$$

such that $C_{V/on}$ is the coarse tuning capacitor bank maximum value and $C_{V/off}$ is the coarse tuning capacitor bank minimum value. To obtain the same *m*-ratio in a switched capacitor topology, the width of the switch has to be reduced to minimize its parasitic capacitance leading to increased losses [37]. Sizing the switch up results in lower resistance at the expense of larger parasitic capacitance, and hence lower *m*-ratio. In other words, the switch is sized independently of the capacitor, and the switched-capacitor *m*-ratio is directly impacted by the switch size, and consequently its series resistance. The comparison holds with technology scaling if both the switch and the varactor are scaled similarly. Although the minimum feature size decreases with technology scaling, foundries do not typically provide models for minimum length varactors. This relaxed scaling of the varactors impedes the improvement of their performance with technology scaling. Fig. 5(a) compares the equivalent parallel resistance ($R_{p,Cv}$) on a 130 nm process of the switched varactors to switched capacitors where the length of the switch (L_{sw}) is fixed at 130 nm while L_{var} is varied. Note that the switched varactors structure has higher $R_{p,Cv}$ than the switched capacitors for L_{var} less than 600 nm at the same *m*-ratio and $C_{V/on(off)}$ value.

A digitally switched varactor structure is utilized in this analysis under the assumption that L_{var} scales with technology. The equivalent parallel resistance of switched varactors ($R_{p,Cv}$) is fitted to

$$R_{p,Cv/on(off)} = \frac{A_{Cv/on(off)}}{f^2 C_{v/on(off)}} \tag{2}$$

where $A_{Cv/on(off)}$ is a fitting parameter and the ON-state is the worst case losses ($A_{Cv/on} = 40 \times 10^9$ Hz, 60×10^9 Hz, 80×10^9 Hz and 100×10^9 Hz for 130 nm, 90 nm, 65 nm and 45 nm processes, respectively). The worst case resistance, $R_{p,Cv/on}$, is noticed to improve significantly with the technology scaling and to degrade sharply with frequency, as depicted in Fig. 5(b).

The fine tuning capacitance represents a very small portion of the overall capacitance. Therefore, its impact on the overall tank *Q*

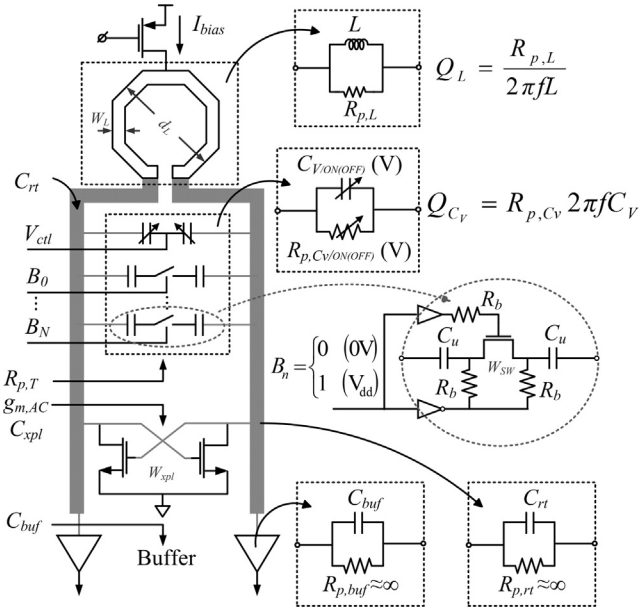

Fig. 1. Top-biased NMOS LC-VCO.

[1] Note that this analysis deems fit to similar differential LC-VCO topologies (e.g., Top/Bottom-Biased NMOS/PMOS/CMOS).

[2] Note that differential values of the LC-tank and cross-coupled pair parameters are assumed throughout this paper.