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Layout-aware design methodology for a 75 GHz power amplifier in a 55 nm SiGe technology

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ABSTRACT

This paper describes a method to design mmW PAs, by modeling the electromagnetic behavior of all the passive structures and the layout interconnections using a 3D-EM solver. It allows the optimization of the quality factor of capacitors (Q-factors > 20 can be obtained at 80 GHz), the access points and arrangement of the power transistor cells. The method is applied to the design and optimization of an E-Band PA implemented in a 55 nm SiGe BiCMOS technology. The PA presents a maximum power gain of 21.7 dB at 74 GHz, with a 3-dB bandwidth covering from 72.6 to 75.6 GHz. The maximum output P1dB is 13.8 dBm at 75 GHz and the peak PAE is 14.1%.

1. Introduction

The recent developments in low cost, high speed CMOS and SiGe BiCMOS technologies, together with the need for multi-gigabit wireless data transmission and security applications have driven intensive research on the development of new millimeter-wave (mmW) circuits and systems using silicon technologies. Most common applications are WiGig (IEEE 802.11ad) and WirelessHD at 60 GHz [1,2], Automotive Radars at 77 GHz [3], E-Band point-to-point links for mobile backhaul networks [4] and mm-wave imaging at 94 GHz [5].

The reduced wavelengths of mmW frequencies allow designers to use distributed elements like transmission lines in a reduced space. However, they also introduce some difficulties such as a lack of accurate simulation models for passive elements (capacitors, transmission lines, inductors…) suitable for mmW frequencies and the need for including the electromagnetic behavior of the layout interconnections in the early stages of the design process. This differs from the design of circuits for lower frequencies, where a post-layout simulation (PLS) extracting the parasitic resistance and capacitance of the layout routing is usually run at the end of the design flow. However, PLS extractions do not usually consider the inductive behavior of the lines, which can significantly compromise the performance of the circuits at mmW frequencies. Therefore, there is a strong motivation for the development of layout-aware design and accurate simulation methodologies for mmW circuits [6,7]. On the other hand, the power amplifier is a key element in any integrated transceiver, especially when high linearity and output power are required.

This paper presents a layout-aware design methodology applied to the design of a mmW PA for the lower E-Band frequencies. It is organized as follows: Section 2 describes the PA circuit and discusses its main elements. Section 3 explains the layout-aware design and simulation procedure, whereas Section 4 presents the measurement results in comparison with simulations, focusing on its gain, bandwidth and compression values. Finally, Section 5 concludes the article.

2. Description of the PA

2.1. Architecture overview

The power amplifier is implemented in a 55 nm SiGe BiCMOS process from STMicroelectronics, which provides 8 metal layers, being two of them thick metals and the last one an ultra-thick metal layer. Most of the mmW PAs are based on 2 identical unit cells which are combined at the output using a balun or a Wilkinson combiner [8,9]. This way, it is possible to achieve a higher output power than with a single cell. In this paper the design of one of these single-ended cells is considered, with the schematic shown in Fig. 1, including all the matching networks and power cells. As it can be observed, the circuit consists of a driver in cascode configuration, to achieve higher gain and

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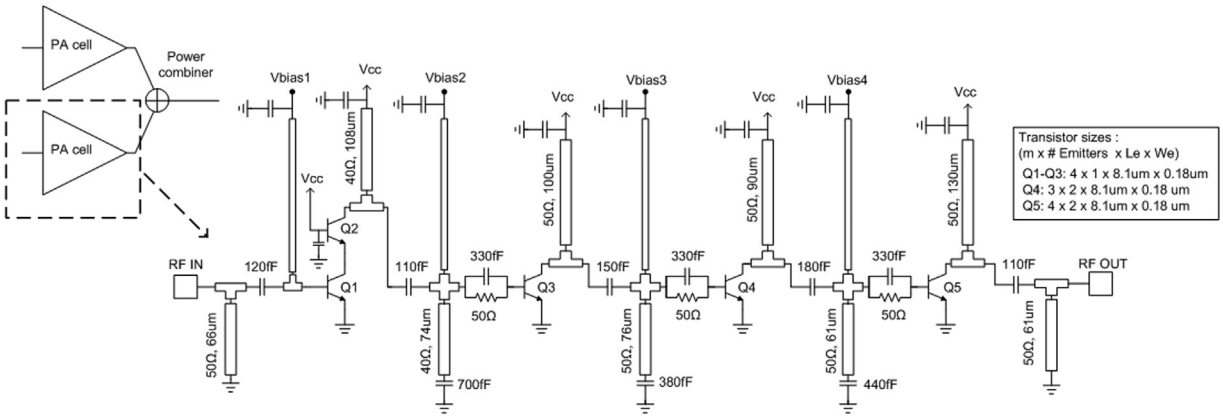

Fig. 1. Schematic of the designed single-ended PA.

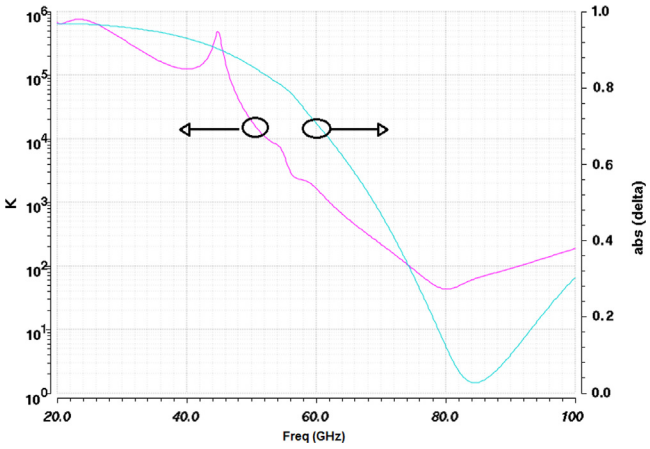

Fig. 2. Simulated K and delta stability factors.

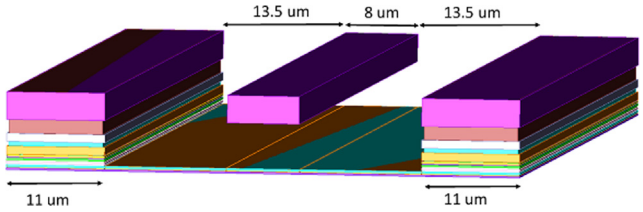

Fig. 3. 3D view of a side-shielded microstrip with dimensions for Zo=50 Ω.

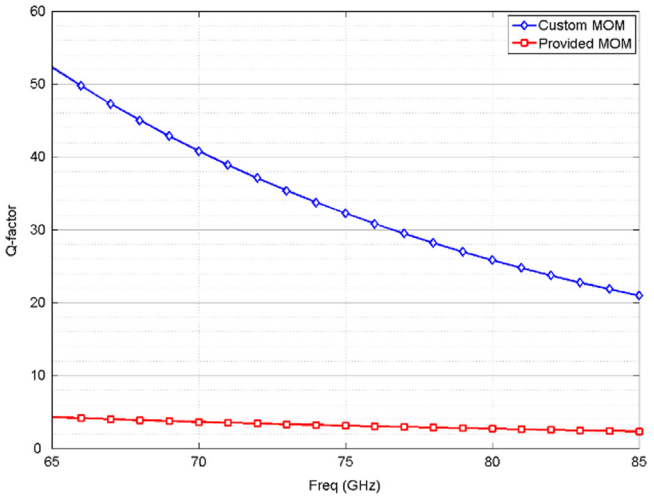

Fig. 4. Q-factor comparison between the custom and conventional MOM capacitors.

stronger input–output isolation, followed by 3 common-emitter stages. Each stage is individually biased, and the biasing points (Vbias1 to Vbias4 in the schematic) are isolated from the mm-wave path by $\sim\lambda/4$ transmission lines and shorted to ground using arrays of big Metal–Oxide–Metal (MOM) capacitors.

2.2. Power transistors

High speed bipolar transistors with f_T/f_{MAX} of 320/370 GHz are selected for the design. They are externally biased using a Vbe value below the one that achieves maximum f_T but which addresses the tradeoff between gain, compression and efficiency, resulting in current densities of 0.3–0.8 mA/μm. The first stages are biased for class A operation, whereas the last stages operate in class AB when drived with high power. A Vcc value of 1.6 V is set in order to avoid breakdown, which is a typical issue due to the low BV_{CE0} usually presented by high speed bipolar transistors in BiCMOS processes. Nevertheless, such limit can be reliably overcome to some extent by designing the matching and biasing networks to present a moderate impedance to the transistor base ($\sim$50 Ω at DC and $\sim$20 Ω at mmW freqs.) [10–14].

The layout of each transistor cell is implemented using multiple parallel emitters to reduce the length to width ratio, whereas the emitter area is increased towards the output stages to increase the output power. Therefore, the total emitter area is 32.4×0.18 μm² for Q1, Q2 and Q3, 48.6×0.18 μm² for Q4 and 64.8×0.18 μm² for Q5.

2.3. Stability

Stability is usually an important issue when designing multi-stage mm-wave power amplifiers, especially when they have single-ended configuration. Additionally, having overall $K\geq1$ and $|\Delta|<1$ is not enough to ensure the unconditional stability of the amplifier under arbitrary source and load impedances. However, as studied in [15], it is also not necessary to ensure unconditional stability of each independent stage, since in the real design they are connected to fixed and known impedances. The approach taken in this design is to analyze the stability of each stage when connected to the stages after it. This is, first the 4th stage is analyzed separately, then stages 3+4 together, afterwards stages 2+3+4 and finally the complete amplifier.