



Active inductor-based tunable impedance matching network for RF power amplifier application



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ARTICLE INFO

Available online 1 August 2015

Keywords:

Active inductor
Power amplifier
Quality factor
Tunable matching network

ABSTRACT

This paper presents the use of a new structure of active inductor named cascoded flipped-active inductor (CASFAI) in a T-type high-pass tunable output matching network of a class-E RF power amplifier (RFPA) to control the output power and enhance the efficiency. The designed CASFAI behaves as an inductor in the frequency range of 0–6.9 GHz, and has reached to a maximum quality factor of 4406, inductance value of 7.56 nH, 3rd order harmonic distortion better than –30 dB for 0 dBm input power, while consumes only 2 mW power. In order to consider the performance of the proposed active inductor-based tunable output matching network on the output power level and power added efficiency (PAE) of RFPA, the CASFAI is applied as a variable inductor to the output matching network of RFPA. The overall circuit is designed and validated in ADS in a 0.18 μm CMOS process and 1.5 V supply voltage. The results indicate that by increasing the inductance value of the matching network in constant operating frequency, the PAE peak moves from high power to low power levels without any degradation. Therefore, it is possible to maintain the power efficiency at the same maximum level for lower input drive levels.

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1. Introduction

Rapid progress in cellular communication and its spread applications have propelled manufacturers of radio transceivers to integrate their products and decrease the number of off-chip elements. Most of blocks forming the wireless communication systems need to be impedance matched with the inputs and/or outputs of other existing blocks in the system, like power amplifier (PA), low noise amplifier (LNA), etc. Power amplifiers are responsible for amplifying the input modulated RF signal before transferring to the antenna. Due to the limited battery life and also its linearity constraints, improving the efficiency of a PA in mobile applications is essentially important [1]. When designing the output matching network of a PA, the output impedance is usually considered constant. However, it is variable most of the time and imposes mismatch conditions to the amplifier, degrading important parameters such as effective output power, efficiency, and phase characteristic. For example, in mobile cell phones, the input impedance of the antenna can be considerably changed by the presence of humans in its vicinity [2]. Furthermore, a mismatch increases the reflection between blocks, and hence, decreases the RF circuit performance, considerably. The impedance

matching network can decrease this reflection, maximizes the transferred power to the load, and also minimizes the returns from the load. The impedance matching occurs at a certain frequency (especially at the resonance frequency) and causes that the maximum power is transferred between the supply and load. For an efficient change in the load impedance of the output stage as a function of desired output power level and also for increasing the total efficiency of the PA, a tunable impedance matching network including one or more elements with tuning capability is needed to obtain a desired impedance value. Furthermore, these matching networks can compensate amplitude and phase distortions produced by transistors. On the other hand, amplifiers usually suffer from efficiency reduction in low power region [3]. Therefore, having an efficiency enhancement strategy for low power operating conditions is mandatory.

Most architectures of tunable impedance matching network insert phase variation to the power gain, meaning that each output power has a different phase, causing AM–PM distortion. This will result in linearity degradation of a PA. One invoked method to overcome this issue is using a constant phase matching network. The T-type high-pass matching network, shown in Fig. 1, consisting of two high-pass LC networks with constant phase characteristic, is considered here as a variable impedance converter, which converts the system impedance Z_0 to the desired load impedance without any phase variation [3].

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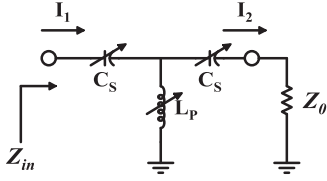


Fig. 1. Configuration of a variable impedance converter using a high-pass T network.

The input impedance and phase difference between input and output currents of the T -type matching network at the resonance frequency, $\omega = \omega_0 = (1/\sqrt{L_P C_S})$, is as follows:

$$Z_{in} = R_{opt} = \frac{L_P}{Z_0 C_S} \text{ \& } \Delta\phi = \frac{\pi}{2} \quad (1)$$

According to (1), at the specified resonance frequency, which corresponds to a constant value for the product of tunable capacitance, C_S , and inductance, L_P , the desired impedance can be varied as a ratio of inductance to capacitance, while the phase difference between the input and output signals is constant ($\pi/2$).

Although, there is a little circuit complexity in the matching networks consisting of passive elements, spiral inductors and variable capacitors (varactors), the tuning range of varactors are limited, while spiral inductors are very bulky with low and fixed inductance, low quality factor and self-resonance frequency, sensitive to temperature variation at high frequencies, and incompatible with low cost standard CMOS processes [4]. Therefore, this paper presents a T -type matching network with gyrator-based active inductor as a tunable matching network for RFPA, which has more advantages in terms of higher quality factor, tunability performance, ability to implement in low cost CMOS processes, and appropriate for reducing size and cost of the chips.

This paper is organized as follows; in section II, the proposed CMOS active inductor employed in the RFPA is introduced. Section III presents the RFPA design procedure with the active inductor-based tunable output matching network and the results are explored. Finally, conclusion is summarized in section IV.

2. Proposed active inductor

The idea of active inductor originates from the theory of gyrator which is based on two back-to-back connected positive and negative transconductors [5,6]. As shown in Fig. 2(a), when the output port of gyrator is loaded by a capacitor, named gyrator-C network, its input impedance shows inductive behavior, as follows:

$$Z_{in} = s \frac{C}{g_{m1} g_{m2}} \Rightarrow L = \frac{C}{g_{m1} g_{m2}} \quad (2)$$

Since the input or output impedances of the transconductors in the gyrator-C network are limited, the synthesized inductor is lossy, meaning that it has parasitic resistance and capacitance. The small signal equivalent circuit of a lossy gyrator-C network can be represented by an RLC network as shown in Fig. 2(b). This means that the circuit has inductive characteristic only in a specific frequency range.

Usually, simple structures are preferred for RF circuits [7–11]. The configuration of basic flipped-active inductor (FAI) introduced in [9] and [10] is very simple and consists of only two transistors. As shown in Fig. 3(a), transistor M_2 located in the forward path has a positive transconductance (g_{m2}) while transistor M_1 in the feedback path provides a negative transconductance (g_{m1}). However, it suffers from low input voltage swing limited to the nMOS threshold voltage minus the overdrive voltage of transistor M_2 ,

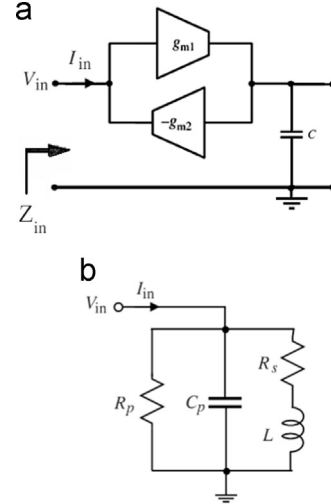


Fig. 2. (a) Gyrator-C network, and (b) equivalent RLC model.

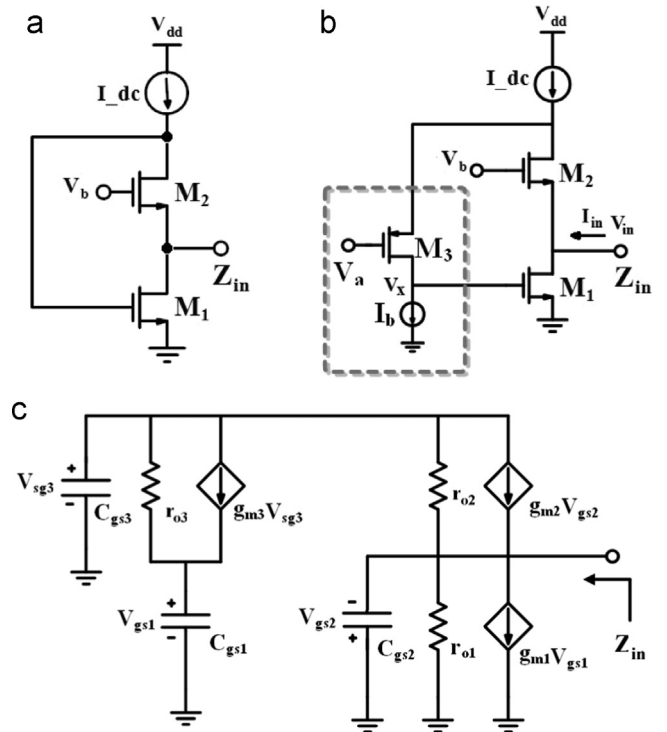


Fig. 3. (a) Basic flipped-active inductor, (b) cascoded flipped-active inductor, and (c) small signal equivalent circuit.

which is not sufficient in most applications and increases non-linearity. Furthermore, this design requires more power consumption to achieve adequate inductance value and high quality factor. In order to overcome these problems, a cascoded flipped-active inductor (CASFAI) presented in [11] is used here for the tunable output matching network of RFPA. In this structure, as shown in Fig. 3(b), a common-gate pMOS transistor M_3 , added in the feedback path, increases the feedback gain and decreases the equivalent series resistance (R_s) of the inductor by a factor of $g_{m3} r_{o3}$, where r_{o3} is the output resistance of the aforementioned transistor M_3 . This leads to an increase in the quality factor of CASFAI in comparison to the conventional FAI. Additionally, the input voltage swing of this architecture can be increased with respect to the conventional FAI, as the drain voltage of M_2 has a value of $V_{D2} = V_{SG3} + V_{G3}$, which can be close to V_{dd} [12]. Moreover,

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