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Noise canceling LNA with gain enhancement by using double feedback

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ABSTRACT

In this paper we present a balun low noise amplifier (LNA) in which the gain is boosted by using a double feedback structure. The circuit is based on a conventional balun LNA with noise and distortion cancelation. The LNA is based on the combination of a common-gate (CG) stage and common-source (CS) stage. We propose to replace the load resistors by active loads, which can be used to implement local feedback loops (in the CG and CS stages). This will boost the gain and reduce the noise figure (NF). Simulation results, with a 130 nm CMOS technology, show that the gain is 24 dB and the NF is less than 2.7 dB. The total power dissipation is only 5.4 mW (since no extra blocks are required), leading to a figure-of-merit (FOM) of 3.8 mW^{-1} using a nominal 1.2 V supply. Measurement results are presented for the proposed DFB LNA included in a receiver front-end for biomedical applications (ISM and WMTS).

1. Introduction

Wireless communications for Industrial, Scientific, and Medical (ISM) and Wireless Medical Telemetry Service (WMTS) applications [1] are found to be low cost, require low power, low voltage transceivers, fully integrated on a single chip [2–4]. The LNA is a key block in these systems and will be investigated in this paper.

Wideband LNAs with high gain and low noise figure (NF), using noise and distortion cancelation have been proposed [5–7], but these circuits have large power dissipation for high gain and low noise figure.

In this paper our main goal is to design a very low area and low cost LNA, with very high gain and low NF using 1.2 V supply. This is obtained by replacing the load resistors by transistors biased close to saturation. In [7] a circuit operating at 1.2 V with controllable gain was proposed. In [8] an LNA with double feedforward (DFF) has been used. In this paper we investigate the possibility of using a double feedback (DFB) technique to boost the gain and reduce the noise figure (NF).

Equations for gain and noise figure are presented, which can be used to optimize the circuit performance. A circuit prototype in a 130 nm standard CMOS technology at 1.2 V has been designed and simulated to demonstrate the proposed technique. Simulation results show a gain of 24 dB and NF below 2.7 dB, with power dissipation of only 5.4 mW, leading to a FOM of 3.8 mW^{-1}, which is, to the authors' knowledge, the best FOM in the literature for LNAs with nominal 1.2 V supply.

Measurement results for the proposed DFB LNA where it is included in a modern receiver are also presented, which prove that the proposed approach leads to a high gain, low NF circuit, when compared with other state-of-the-art approaches.

2. Balun LNA with noise cancelation

In a receiver, the antenna and RF filters are typically single-ended, so it is very desirable to have an LNA with single-ended input. A differential signal in the receiver is preferred to reduce harmonic distortion and to reject power supply and substrate noise [6]. Traditionally, an external balun is used to convert single-ended signals to differential, but it introduces losses and degrades the receiver NF. A balun LNA converts a single-ended to a differential signal, which simplifies the receiver design, by avoiding the external balun [6].

The circuit proposed in [6] and shown in Fig. 1 is a balun LNA, in which the thermal noise of M_1 (main source of noise) is canceled out. The noise produced by M_1 appears in phase at the two output terminals, while the signals at these terminals are in opposition. Thus, at the differential output the gain is doubled and the noise is canceled. It can be shown [6] that the distortion introduced by M_1 is also canceled.

The differential voltage gain of the LNA is obtained from the difference of the common-gate (CG) and the common-source (CS) stage gains:

$$A_{v,Diff} = g_{m1}(R_1 \backslash\backslash r_{ds1}) + g_{m2}(R_2 \backslash\backslash r_{ds2}) \quad (1)$$

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where r_{ds} is the transistors output resistance and g_m is the transconductance. The input impedance is given, approximately, by

$$Z_{in} = \frac{1}{g_{m1}} \tag{2}$$

3. Proposed circuit

The circuit in Fig. 1 cannot operate at low supply voltage with high gain, due to the large voltage drop at the resistors. Based on the CG–CS LNA circuit of Fig. 1, we investigate a circuit using active loads, in which the load resistors are replaced by transistors biased in the triode region, which behave, approximately, as linear resistors [7].

In [8], a method was proposed to obtain gain boosting in the LNA of Fig. 1, which was referred to as double feed-forward (DFF) LNA, since it consisted of the use of two feed-forward loops, as shown in Fig. 2.

Since the CG stage gain is limited by the input matching, an inverter based block with gain α is applied (this inversion is required, since the CG stage does not change the input signal phase) in the feedforward path. This modification provides gain boosting and an additional degree of freedom in the design. At the same time the input signal is also applied at CS stage through a feedforward loop, but in this case there is no need of an inverter, and the CS gain can be adjusted through V_{b2}. Despite the significant gain boosting this circuit provides, its linearity and bandwidth are degraded. Here we propose an alternative method of gain boosting, which uses two local feedback loops as shown in Fig. 3. This circuit will be referred to here as double feedback (DFB) LNA. A DFB LNA is a simpler circuit than DFF LNA (hence, with lower area and power), and produces a higher gain increase and more NF reduction.

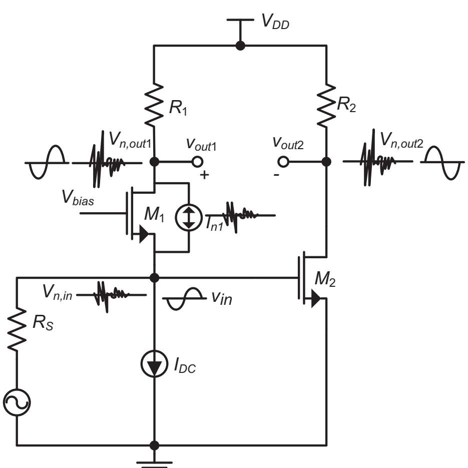

Fig. 1. Balun LNA with canceling of the noise of the CG-transistor M_1 [6].

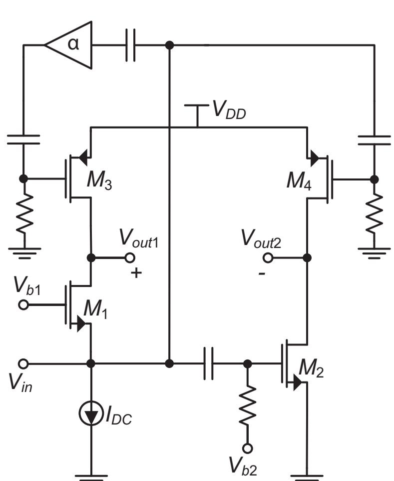

Fig. 2. LNA using double feedforward (DFF) [8].

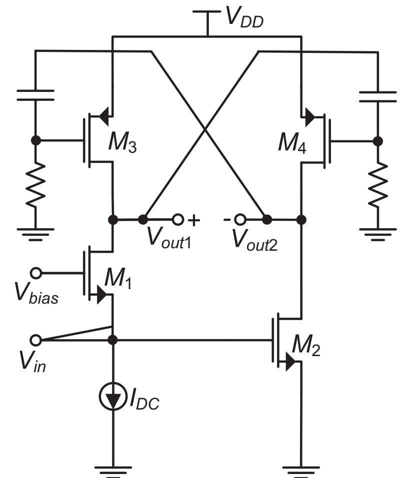

Fig. 3. Proposed LNA using double feedback (DFB).

In the DFB LNA (Fig. 3), V_{in} after amplification in the CG stage (M_1) is applied to the gate of M_4, being further amplified and added to V_{out2}. The resulting signal is amplified trough M_3, and added to V_{out1}. With this structure there is a significant gain increase, without using extra circuitry.

In the proposed circuit the main drawback is the reduction of the bandwidth due to the parasitic capacitances of M_3 and M_4, but the main goal is achieved: high gain and low NF.

The PMOS loads could be biased under saturation, which would lead to a higher gain due to the increase of the channel resistance. However, the circuit would be sensitive to DC variations, requiring a common-mode feedback (CMFB) type regulation circuit to compensate these variations, and consequently, adding more complexity to the circuit. Moreover, in the presence of mismatches, noise cancelation is still partially canceled, but distortion cancelation will be severely degraded [9].

The gain of the CG and CS stages is

$$\frac{V_{out1}}{V_{in}} = \frac{g_{mCG} g_2 + g_{m2} g_{m3}}{g_1 g_2 - g_{m3} g_{m4}} \tag{3}$$

$$\frac{V_{out2}}{V_{in}} = -\frac{g_{m2} g_1 + g_{mCG} g_{m4}}{g_1 g_2 - g_{m3} g_{m4}} \tag{4}$$

where $g_1 = g_{ds1} + g_{ds3}$ and $g_2 = g_{ds2} + g_{ds4}$.

Using (3) and (4), we obtain the LNA differential gain:

$$A_{v,Diff} = \frac{V_{out1} - V_{out2}}{V_{in}}$$

$$= \frac{gmCG(g_{m4} + g_2) + g_{m2}(g_{m3} + g_1)}{g_1 g_2 - g_{m3} g_{m4}} \tag{5}$$

The input impedance is

$$Z_{in} = \frac{g_1 g_2 - g_{m3} g_{m4}}{g_{mCG}(g_2 g_{ds3} - g_{m3} g_{m4}) - g_{m2} g_{m3} g_{ds1}} \tag{6}$$

Using Eqs. (5) and (6), we can optimize the circuit performance in order to increase the gain, while minimizing the impact on the input matching.