INTEGRATION, the VLSI journal 52 (2016) 1–9

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Surrogating circuit design solutions with robustness metrics

Jin Sun [a,b,*], Liang Xiao [a], Jiangshan Tian [a], He Zhou [b], Janet Roveda [b]

[a] School of Computer Science and Engineering, Nanjing University of Science and Technology, No. 200 Xiaolingwei Street, Nanjing 210094, China
[b] Department of Electrical and Computer Engineering, The University of Arizona, 1230 E. Speedway Blvd., Tucson 85721, USA

ARTICLE INFO

Article history:
Received 28 January 2015
Received in revised form
16 May 2015
Accepted 27 July 2015
Available online 8 August 2015

Keywords:
Robust design
Robustness metric
ElasticR method
Surrogates
Process variations

ABSTRACT

With the increase in device variability, the performance uncertainty poses a daunting challenge to analog/mixed-signal circuit design. This situation requires a robust design approach to add large margins to the circuit and system-level specification to ensure correct operation and the overall yield. In this paper, we propose a new robust design approach by using norm metrics to quantify the robustness for both design parameters and performance uncertainty. In addition, we adopt a surrogating procedure to achieve robustness in design space and to reduce uncertainty in performance space. The end result of the proposed method is a Pareto-surface that provides the designer with trade-offs between design robustness and performance uncertainty. One advantage of this new approach is the ability to take into account the strong nonlinear relationship between performance and design parameters. Considering a set of highly nonlinear circuit performances, we demonstrate the effectiveness of this robust design framework on a fully CMOS operational amplifier circuit.

1. Introduction

The continuous decrease of CMOS device size leads to the increase in the process variations. With the increase in device variability, the performance uncertainty poses a daunting challenge to circuit design. For instance, a 5% variation in transistor channel length may introduce up to 10× difference in leakage current and even causes functional failures in mixed-signal circuits [1–3]. Traditional approaches, such as timing analysis and yield estimation techniques [4–6], generally model circuit performance as a function in terms of design parameters. These parameterized models estimate performance fluctuations relying on the uncertainties in design parameters. It becomes apparent that the increasing device variability requires adding large margins to the circuit and system-level specification to ensure correct operation as well as the overall yield. Indeed, the ability to facilitate flexible designs is the key to improving circuit quality.

To ensure a safe, invulnerable design, it is of great importance to develop a design framework that is robust to parameter variations, and thus provides the designer with enough design margin. One popular methodology to improve circuit quality is robust design. This methodology focuses on simultaneously reducing parameter intervals and improving the fundamental functions of circuits or systems, and thus helps variable designs and concurrent engineering [7,8]. Over the past decades, many academic groups and companies are involved in traditional Taguchi method [9–13]. These efforts have had great impact on improving design quality and reducing design cost. However, many of them have reached the maximum potential due to their overly pessimistic nature.

Recently, several new attempts have been made for robust design. One category approaches use either design space exploration or norm concept to demonstrate design robustness. For example, [14] created an optimization methodology for generating a robust Pareto surface based on fast Monte-Carlo analysis. Ref. [15] proposed a norm-based metric to quantify design robustness in statistical timing analysis. This work predicts design parameter space in a backward mapping fashion. However, [15] does not provide a feasible optimization procedure for improving design robustness. On the other hand, a lot of efforts have been made to formulate robust design under parameter variations as a set-based deterministic problem. These methods generally employ a uncertainty set to capture the variability in design parameters. The resulting set-based design problem can be further reduced to a deterministic one by constructing a solution that is robust to the variations within the uncertainty set. For example, the ellipsoidal uncertainty model [16,17] is widely used to characterize parameter variations as a deterministic ellipsoidal set. Ref. [18] further proposes a conic representation of uncertainty set, of which the size are associated with not only the nominal design point, but also the specified yield

* Corresponding author at: School of Computer Science and Engineering, Nanjing University of Science and Technology, No. 200 Xiaolingwei Street, Nanjing 210094, China.
E-mail addresses: sunj@njust.edu.cn (J. Sun), xiaoliang@njust.edu.cn (L. Xiao), 912106840410@njust.edu.cn (J. Tian), hezhou@email.arizona.edu (H. Zhou), meilingw@email.arizona.edu (J. Roveda).

http://dx.doi.org/10.1016/j.vlsi.2015.07.015
0167-9260/

requirement. All these set-based approaches assume that an explicit and accurate model of circuit performance has been established before solving the optimization problem.

In many scenarios, the objective and constraint functions in robust design framework are implicit and expensive, due to the increasing complexity of integrated circuits. To tackle this problems, surrogate models are widely researched to approximate circuit performance based on cost-effective model templates. Surrogate models are built on sampling data obtained from SPICE-like simulations. Response surface model (RSM) is a traditional method widely used in circuit performance modeling. However, RSM is incapable of capturing the strong nonlinearity of circuit performance upon parameter variations. Moreover, RSM requires a huge number of samples when constructing the surface model. In recent years, more researches have been conducted to develop other powerful surrogate models, including Kriging, rational and radial basis functions [19–21]. For example, [19] proposes using Kriging model combined with Latin Hypercube Sampling to build a reasonable surrogate model of circuit performance.

Above existing approaches model circuit performance as a linear or piece-wise linear function in terms of design parameters. Therefore when evaluating highly nonlinear circuit performances, such as gain-bandwidth, and phase margin, these approaches fail to capture the nonlinear relationships between performances and design parameters, and tend to predict non-robust design solutions. Despite its growing importance in today's circuits and applications, achieving robustness with highly nonlinear circuit performances has not been addressed enough by existing researches. Such cases observe major performance shifts with very insignificant parameter variations, and thus demand limiting performance uncertainty while allowing maximum robustness for design parameters.

In this paper, we propose a new robust design framework that includes both forward mapping and backward mapping procedures. We consider a set of circuit performances with nonlinear/implicit function expressions of design parameter. Starting with user-defined performance constraints, we first apply backward mapping [22–24] to identify feasible regions for design parameters. Then we propose an ElasticR method to measure the norm distance from the nominal design solution to any design points that will cause performance violation. The minimum distance thus generated demonstrates the robustness for design parameters. In addition, a forward mapping procedure [25,26] is applied to measure the robustness for performance fluctuations induced by parameter variations. Similarly, we measure the maximum norm distance between nominal performance point and performance fluctuations. After quantifying the robustness metrics in both parameter space and performance space, we then identify optimal nominal design parameters that have the maximum robustness while minimizing performance fluctuation. This optimization procedure is implemented by employing surrogating techniques [27,28] to efficiently search for optimal design solutions. The contributions of this paper include: (1) proposing a two-way mapping procedure to ensure robustness for design parameters and performance variations, (2) developing an ElasticR method of robustness quantification to estimate design parameter boundaries as well as their associated performance boundaries, and (3) providing surrogate-based optimization procedure to iteratively search optimal design solutions among a group of candidates. The proposed methodology was verified on an analog operational amplifier circuit. Experimental results show that this two-way mapping approach has achieved an up to 38% robustness improvement compared with one-way mapping procedures.

The rest of this paper is organized as follows. Section 2 defines two robustness metrics both in parameter space and performance space based on norm distance. Section 3 details the surrogate-based robust design framework for robustness metrics. Experimental results are presented in Section 4. Finally, Section 5 concludes this paper.

2. Quantifying robustness for parameter and performance

This section introduces two robustness metrics in both parameter space and performance space. An ElasticR method is developed for the quantification of both robustness metrics.

2.1. Parameter robustness

Consider a group of design parameters $L_{\text{eff}1}, W_1, T_{\text{ox}1}, L_{\text{eff}2}, W_2, T_{\text{ox}2}, \ldots$, representing effective channel length, width, oxide thickness for each device. To simplify the notation, we use vector $X=(x_1, x_2, \ldots, x_n)$ to represent all design parameters, with parameter variations ΔX around their nominal values X^0. Denoted by $Y=(y_1, y_2, \ldots, y_m)=f(X)$, the corresponding circuit performances may include gain-bandwidth, phase margin, slew rate and other performance metrics. Likewise, Y^0 and ΔY represent the nominal performance metrics and the corresponding perturbations.

In robust design, there exist performance limits, $Y^L=(y_1^L, y_2^L, \ldots, y_m^L)$ and $Y^U=(y_1^U, y_2^U, \ldots, y_m^U)$, such that the fluctuations in circuit performance due to parameter variations satisfy

$$y_j^L \le \Delta y_j = y_j - y_j^0 \le y_j^U, \quad j=1,\ldots,m \tag{1}$$

where y_j^L and y_j^U indicate the maximum acceptable fluctuations for j-th circuit performance. On the other hand, parameter variations also have lower bound X^L and upper bound X^U that come from design rule requirements. In general, the values of X^L and X^U may vary depending on the location of nominal design in parameter space.

A good design should satisfy that design parameters lead to performances bounded by the performance specifications. We define feasible region as a set in parameter space consisting of all design candidates that produce performance metrics satisfying the performance constraints. In other words, the performance constraints map backward into parameter space and form a parameter feasible region. Note that design parameters the mselves are limited by their variation bounds X^L and X^U. In a rigorous manner, for any design candidate X^0 whose robustness to be evaluated, considering parameter variations and performance constraints, there will be a set of acceptable variations in parameter space, such that the performance fluctuations propagated from this set will not violate the performance constraints:

$$\text{FR}=\left\{\Delta X \,|\, Y^L \le \Delta Y \le Y^U,\ X^L \le \Delta X \le X^U\right\} \tag{2}$$

where Y^L and Y^U represent the performance specifications, and ΔY denotes the performance perturbations due to parameter variations: $\Delta Y = f(X^0+\Delta X) - f(X^0)$. The region defined in (2) includes all feasible parameter variations that satisfy performance constraints, and therefore is named as parameter feasible region (FR). Fig. 1 shows an example of a FR in a 2-dimensional parameter space. We observe that FR is specified by both parameter variation bounds and performance specifications. A point inside FR (Point A) or on the boundary of FR (Point B) represents a feasible variation value that satisfies the performance constraints. On the other hand, a point outside FR represents a perturbation value that violates the performance constraints (Point C), or exceeds parameter variation range (Point D).

We suggest using a distance-based metric to quantify the robustness for design parameters within the feasible region. Norm distance is beneficial to describing the large dimensionality of