

Formation of 10–30 nm SiO₂/Si structure with a uniform thickness at ~120 °C by nitric acid oxidation method

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Abstract

Silicon dioxide (SiO₂) layers with a thickness more than 10 nm can be formed at ~120 °C by direct Si oxidation with nitric acid (HNO₃). Si is initially immersed in 40 wt.% HNO₃ at the boiling temperature of 108 °C, which forms a ~1 nm SiO₂ layer, and the immersion is continued after reaching the azeotropic point (i.e., 68 wt.% HNO₃ at 121 °C), resulting in an increase in the SiO₂ thickness. The nitric acid oxidation rates are the same for (1 1 1) and (1 0 0) orientations, and n-type and p-type Si wafers. The oxidation rate is constant at least up to 15 nm SiO₂ thickness (i.e., 1.5 nm/h for single crystalline Si and 3.4 nm/h for polycrystalline Si (poly-Si)), indicating that the interfacial reaction is the rate-determining step. SiO₂ layers with a uniform thickness are formed even on a rough surface of poly-Si thin film.

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1. Introduction

Si/silicon dioxide (SiO₂) structure attracts much interest not only from academic viewpoint but also for technological application to semiconductor devices such as large scale integration (LSI) and thin film transistors (TFT). In the case of TFT using poly-crystalline Si (poly-Si) thin films, the formation of relatively thick gate SiO₂ layers (i.e., ~50 nm) is required. This is because (i) the conventional method (i.e., plasma-enhanced chemical vapor deposition (PECVD) using tetraethylorthosilicate (TEOS)) [1–7] cannot form uniform SiO₂ layers on rough poly-Si surfaces which result from laser annealing of amorphous Si films to

crystallize [8], and (ii) the deposition method cannot form high quality dense SiO₂ layers. Thick gate SiO₂ layers increase a threshold voltage, resulting in an increase in the power consumption. Moreover, the deposition methods result in poor interfacial characteristics (e.g., high interface state density) because of incomplete interfacial bond formation, incomplete cleaning of poly-Si surfaces before deposition, etc [1–3]. The SiO₂ layers fabricated from TEOS include water, hydroxyl species, and carbon species, which increase the leakage current density [1,2]. The leakage current density also increases with a decrease in the deposition temperature [3]. To improve the electrical characteristics of the SiO₂ layers formed from TEOS, low pressure deposition [1], low deposition rate [4], NH₃ plasma treatment [5], N₂O plasma treatment [1], multi-layers fabrication [6,7], etc., have been employed.

Several methods have been investigated to form SiO₂ layers at low temperatures, e.g., plasma oxidation [9,10],

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metal-promoted oxidation [11,12], and ozone oxidation [13]. However, the low temperature formation of thick SiO₂ layers with good electrical characteristics has not been successful.

We have recently developed a nitric acid oxidation of Si (NAOS) method to form SiO₂ layers at ~120 °C [14–18]. The NAOS method is a direct Si oxidation method in which oxygen atoms formed by decomposition of nitric acid (HNO₃) react with Si. Consequently, the SiO₂/Si interface is clean, leading to good interfacial characteristics. Ultrathin (i.e., ~1.3 nm) SiO₂ layers formed with 68 wt.% HNO₃ (i.e., azeotropic mixture with water) have a much lower leakage current density than those for thermally grown SiO₂ layers, and possess a high atomic density of 2.34×10^{22} atoms/cm³ (i.e., ~3% higher than that of thick thermal SiO₂ layers), preventing further growth of the SiO₂ layers [14–16]. We have recently found that a two-step NAOS method (i.e., immersion in ~40 wt.% HNO₃ followed by the immersion in 68 wt.% HNO₃), on the other hand, can form thicker SiO₂ layers [18].

In the present study, the two-step NAOS method has been applied to form SiO₂ layers with thickness more than 10 nm on single crystalline Si and poly-Si. The oxidation rate is found not to depend on the Si surface orientations and the conduction types, and uniform thickness SiO₂ layers can be formed even by oxidation of poly-Si thin films with a rough surface.

2. Experiments

Phosphorus-doped n-type or boron-doped p-type Si wafers having (111) or (100) orientation were used for the substrates. Intrinsic poly-Si films with ~50 nm thickness deposited on glass by means of the PECVD method were also employed for the substrates. After cleaning these Si specimens using the RCA method, the specimens were immersed in 40 wt.% HNO₃ aqueous solutions at the boiling temperature of 108 °C. The boil of the HNO₃ solutions increased the concentration to 68 wt.% (i.e., azeotropic mixture with water) [15], and after reaching the azeotropic point, immersion in the azeotropic mixture was continued for various periods. The metal impurity concentration in the HNO₃ solutions employed in the present study was less than 1 ppb. The resistivity of water used was 18.2 MΩ cm.

X-ray photoelectron spectroscopy (XPS) measurements were performed using a VG Scientific Escalab 220i-XL spectrometer with a monochromatic Al Kα radiation source. Photoelectrons were collected in the surface-normal direction. Ellipsometry measurements were performed using a Sopra GES-5 ellipsometer. Transmission electron micrographs (TEM) were observed using a JEOR JEM-3000F apparatus.

3. Results and discussion

Fig. 1 shows XPS spectra in the Si 2p region for the SiO₂/Si(100) structure formed by the NAOS method.

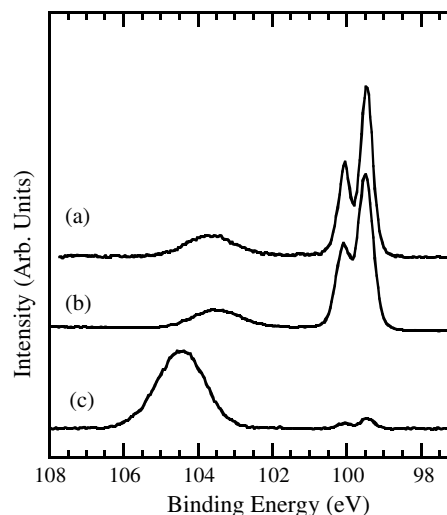


Fig. 1. XPS spectra in the Si 2p region for the SiO₂/Si(100) structure formed by the NAOS method. Si wafers were immersed (a) in 68 wt.% HNO₃ at 121 °C for 15 h, and in 40 wt.% HNO₃ at 108 °C and the immersion was continued for the following periods after reaching the azeotropic point: (b) 0 h; (c) 15 h.

Doublet peaks were due to Si 2p_{3/2} and 2p_{1/2} levels of the Si substrate and a broad peak in the higher binding energy region was due to the SiO₂ layers. The thickness of the SiO₂ layers was determined from the intensity ratio between the SiO₂ peak and the substrate peaks [19], using 3.2 nm as the mean free path of photoelectrons in SiO₂. Using this mean free path value, XPS measurements give nearly the identical SiO₂ thickness to that estimated from ellipsometry measurements when the SiO₂ thickness is larger than ~4 nm. By the immersion of Si in 68 wt.% HNO₃ (i.e., azeotropic mixture of HNO₃ with water) at its boiling temperature of 121 °C, an ultrathin SiO₂ layer of ~1.4 nm thickness was formed during 10 min immersion [14,15] but its thickness did not increase even when the immersion was kept for 15 h (spectrum a). When Si was immersed in 40 wt.% HNO₃ at the boiling temperature of 108 °C and the boiling was kept for 15 h after reaching the azeotropic point, on the other hand, the SiO₂ thickness increased to 14.4 nm (spectrum c). In this case, it took ~1 h to reach the azeotropic point from 40 wt.% HNO₃, and at this point, a 1.1 nm SiO₂ layer was formed (spectrum b). The energy difference between the SiO₂ peak and the substrate Si 2p_{3/2} peak was 3.9 eV for the 1.1 nm SiO₂ layer, and it increased with the SiO₂ thickness. This higher energy shift is attributable to an increase in the magnitude of charging, resulting in an increase in the potential drop across the SiO₂ layer [20,21].

XPS measurements show that the SiO₂ layers formed by the two-step NAOS method are almost stoichiometric, i.e., Si:O = 1:2 ± 0.05. In spite of the stoichiometric SiO₂ layers, diffusion of the oxidizing species (most probably oxygen atoms) proceeds smoothly due to the small size, as explained below.

Fig. 2 shows the thickness of the SiO₂ layers formed on the Si(100) substrates (plot a) and poly-Si thin films (plot

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