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Substrate noise isolation improvement in a single-well standard CMOS process

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ABSTRACT

This work describes a fully CMOS compatible methodology, which makes available a pseudo deep n-well in single-well standard CMOS process. The proposed method is based on mask manipulation to accommodate the field implant p-type region into the n-well, and does not require any additional masks or modification in the CMOS process flow. According to the experimental results, the floating NMOS made available by the methodology shows a reduction in the threshold voltage, which implies a slight improvement in its performance, when compared with its standard NMOS counterpart. It was also experimentally demonstrated up to 3 GHz, that the guard-ring field implant/pseudo deep n-well proposed structure improves substrate noise isolation when compared to the classical p+ guard-ring, with a maximum improvement above 20 dB for low frequencies and a minimum of 4 dB at 3 GHz.

1. Introduction

As CMOS technology continues its scaling down to the nanometer range, processing is also becoming more complex, with an increasing number of masks and related processing steps. Modern ICs include a diversity of digital, analog, mixed-signal and radio-frequency (RF) functional blocks, with different power, bias levels and signals of different frequencies, sharing the same CMOS die. Also, very high frequency digital and power management parts are responsible for the increase of the noise level in the IC, which can seriously affect the performance of sensitive analog and RF parts, like band-gap references, low-noise amplifier and oscillator circuits.

To circumvent these problems, CMOS technology has evolved, not only above Silicon (e.g., thinner dielectrics, low and high k dielectrics, increased number of metal levels and accessibility to thick Copper layers), but also at Silicon level, with the availability of trench isolation structures, multiple well processes and, in some specific cases, buried layers.

CMOS processes including a deep n-well are available to circuit designers from, at least, a decade ago [1]. Some works report that deep n-well regions can be used to improve substrate noise isolation [1–6] and devices performance, namely, increase of the cutoff and maximum oscillation frequencies [1,6], and reduction of harmonic distortion [7]. Furthermore, deep wells are widely used in the development of high-voltage (HV) devices in HV CMOS [8–11] and in CMOS compatible photodiode and phototransistors structures, aimed at optical and communication applications [12–14].

For some applications, where layout area is not the major concern, designers can still resort to 'older' technology nodes (> 180 nm), if functionality versus Silicon footprint trade off becomes acceptable, especially at the prototyping stage. However, the deep n-well formation is not available in those CMOS processes. In that case, circuit design could become unviable if applications requiring different reference levels and ground floating devices are in scope.

In this work a fully CMOS compatible methodology is used to create a p-type isolated region inside the single n-well, resorting to the p-type field implantation available in the process. The idea is to adapt the concept of the deep n-well and bring its advantages to single-well CMOS processes, with the associated advantages, like the availability of floating circuits (different references, not connected to the die p-type substrate), and correlated substrate noise cross-talk reduction. In this way, these processes, which are poor in features when compared to recent nodes with multiple wells, becomes enriched in functionality.

Section 2 describes the mask manipulation methodology to achieve the isolated lightly doped p-type region inside the standard n-well, without any modification in the fabrication steps of the CMOS process. In Section 3 the proposed methodology is validated throughout experimental results. In Section 4,

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experimental results also demonstrate that these field implanted isolated regions can be used to significantly reduce substrate noise propagation. Finally, in Section 5, some conclusions are drawn.

2. The design of the isolated p-type region

The complete envelopment of a lightly doped p-type region inside an n-well region is an obvious task in a triple well CMOS process, due to the availability of the deep n-well. In these cases, the isolated region will be formed by a p-well implant over the pre-processed deep n-well [1,6,8,10,11].

In single well CMOS processes this possibility is not considered. In fact, basic CMOS processing is founded on two basic requirements: a p-type substrate (p-sub) that forms the bulk of the NMOS transistors; and the presence of an n-well to act as the local bulk for the complementary PMOS transistors. Fig. 1a shows the part of the typical mask arrangement used for the layout design of the complementary pair (n+, p+ and contact masks not shown, for simplicity). In general, a shallow p-type region is formed in all those regions where n-well is not present. This p-type implant is usually denoted as field implant or P-block region, and it serves, not only to increase parasitic devices threshold voltage, but also to increase the bulk concentration of the standard NMOS transistors. This region is always shallower than the n-well. Depending on each CMOS processing rules, this p-type region is usually defined by an automatic mask generation algorithm, in order to be implanted wherever n-well is absent. For the CMOS process described in Fig. 1a, the automatic mask tool will generate a field implant layout layer (FIMP) coincident with the n-well layout layer (NW). Since the former has a dark field mask, field implantation will only be processed in regions not covered by the field implant layout layer, i.e., those regions without n-well. Similar relations between these layers can be found for the case of other CMOS processes.

This work proposes and discusses the validity of implanting a field implant region with its volume completely surrounded by the n-well pre-processed region. Taking into account that field implant is shallow than the n-well, it is possible to consider its complete immersion in the n-well, as long as the correspondent layout layers are manipulated accordingly. The proposed mask modification is depicted in Fig. 1b. The figure shows that a field implant mask-opening (NOT [FIMP]) window is cut and left covered by the same n-well mask layout. During processing, after n-well formation according to the NW layer, this opening in the field implant mask will allow acceptor ion penetration only in the (NOT[FIMP]) defined window, forming an isolated lightly doped p-type volume. As can be seen, this p-type volume is completely enclosed by the n-well volume, which can be considered as a pseudo deep n-well.

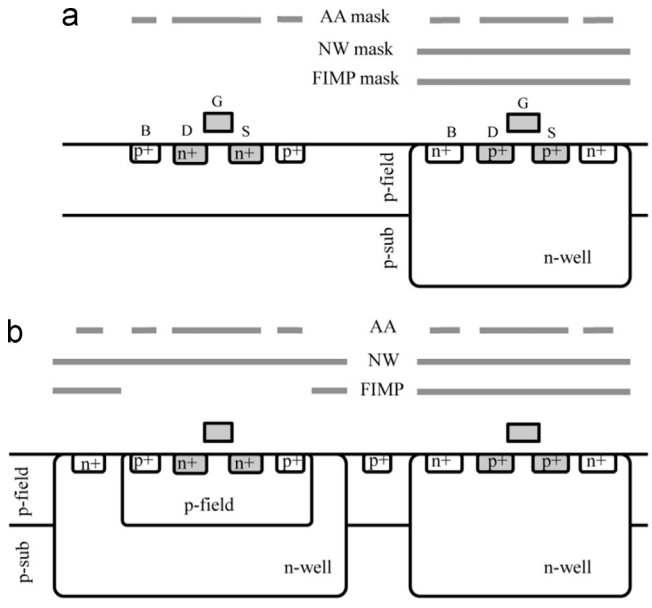

Fig. 1. Cross sections of the structures under study, showing the proposed masks arrangements: (a) The conventional NMOS/PMOS complementary pair; and (b) the "opening" in the FIMP mask layer (left) for the formation of a field implant region inside the pre-processed n-well, to accommodate a floating NMOS.

Fig. 1b shows the implementation of a floating NMOS in this p-type isolated region, showing the junction isolation between the n-well and the p-field (at left) to form the proposed floating NMOS.

This work gives particular emphasis to the designer point of view. In fact, for fabless design houses, or in the case of research works, where prototyping cost is critical, this methodology can overcome the necessity for extra masks or an expensive CMOS process. Like in CMOS processes with an available deep n-well, this proposal permits the fabrication of complete and isolated analog, digital or mixed mode circuits inside this pseudo deep n-well. The methodology is only appropriate to single-well CMOS processes and becomes, of course, superfluous in processes where the deep n-well is already available as a regular mask.

3. Standard and floating NMOS characterization

One of the objectives of the proposed methodology is to achieve a floating NMOS device, with its bulk formed by the p-type field implant present in the CMOS process. The viability of designing such MOSFET and the evaluation of its performance is discussed in this Section. For comparison purposes two geometrically identical NMOS devices were designed and fabricated in a single-well standard CMOS process. Both devices have a channel width and length of $W=5\,\mu m$ and $L=0.35\,\mu m$, respectively. Besides the differences in the field implant (FIMP) and active area (AA) masks, the remaining masks (NW, n+ implants, contacts and metal interconnections) were kept exactly identical. The characterization of both devices was achieved with an Agilent 4156C Semiconductor Parameter Analyzer.

Fig. 2 shows the experimental $I_D(V_{GS})$ characteristics, obtained with $V_{DS}=0.1$ V, for the standard NMOS and the proposed floating NMOS. It can be noticed that the floating NMOS current is higher than the standard NMOS current, even if this difference is almost negligible at strong inversion. However, in the subthreshold region, devices characteristics differences are significant. This difference is also relevant at cutoff, when the samples are exposed to light. In these conditions, the leakage current for $V_{GS}<0$ V present a flat, V_{GS} independent, behavior, but the value in the standard NMOS is almost a decade above the proposed floating NMOS. For the die samples measured in dark, both devices have

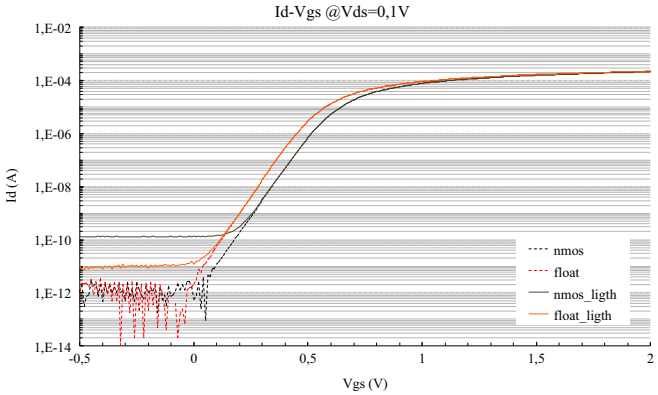

Fig. 2. Comparative experimental $I_D(V_{GS})$ characteristics, for $V_{DS}=0.1$ V, with the die sample in dark and with direct light.