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# A low-power fast tag comparator by modifying charging scheme of wide fan-in dynamic *OR* gates

Mahshid Nasserian [a,*], Mohammad Kafi-Kangi [a], Mohammad Maymandi-Nejad [a], Farshad Moradi [b]

[a] Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
[b] Integrated Circuits and Electronics Laboratory (ICE-LAB), Department of Engineering, Aarhus University, Denmark

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ABSTRACT

In this paper, a new charging scheme for reducing the power consumption of dynamic circuits is presented. The proposed technique is suitable for large fan-in gates where the dynamic node discharges frequently. Simulation results demonstrate that the proposed method is efficiently controlling the internal voltage swing and hence decreasing the power consumption of the wide fan-in *OR* gate without sacrificing other circuit parameters such as gate speed, area or noise immunity. The power-delay product of a simulated 8-input *OR* gate is reduced by 46%, compared to its conventional dynamic counterpart in the 90 nm CMOS technology. Another important benefit of the proposed approach is 99X reduction in power dissipation of the gate load by limiting its switching activity. Furthermore, the delay of the proposed circuit experiences only 0.94% variation over 10% fluctuation in the threshold voltages of all transistors for a 32-bit *OR* gate. Using the proposed technique, a 40-bit tag comparator is simulated at 1 GHz clock frequency. The power consumption of the designed circuit is as low as 1.987 μW/MHz, while the delay and unity noise gain (UNG) of the circuit are 244 ps and 499 mV, respectively.



## 1. Introduction

Digital dynamic circuits provide higher speed and are more area efficient compared to static CMOS circuits and have been the subject of many researches [1–5]. In case the fan-in of a gate is large, the dynamic structure becomes more attractive for high-speed datapath designs. For example, in a 40-bit tag comparator, an *OR* gate with a fan-in of 80 is employed. If this wide fan-in *OR* gate is to be realized by the static structure, the number of transistors that should be stacked will be impractically large. However, wide fan-in dynamic gates are very power hungry in the active mode due to the fact that the capacitance of the dynamic node is very large and it discharges in almost every clock cycle. Furthermore, dynamic circuits suffer from lower noise margin (that is about threshold voltage of the NMOS transistor in footless structures) in comparison to static logic. To improve the noise-immunity of such circuits, different approaches have been proposed [1,6]. Wide fan-in *OR* gates are extensively used in multiplexers [6], tag comparators [7], register files [8], tag match comparator [9], SRAM pre-decoder gate [10], programmable logic arrays (PLA) [11], and programmable encoders [12].

Fig. 1 shows the structure of the conventional dynamic logic. As shown in this figure, $M_p$ charges the dynamic node (i.e. *Dyn*) to $V_{DD}$ at the precharge phase ($CLK=0$). In case the pull-down network (PDN) is off in the evaluation phase ($CLK=1$), the voltage of dynamic node remains at $V_{DD}$; otherwise the dynamic node discharges to ground. In wide fan-in dynamic *OR* gates, the PDN is a parallel combination of *N* transistors. Therefore, the voltage on the dynamic node may drop due to the leakage current through NMOS transistors of PDN block and other noise sources such as crosstalk and supply noise that becomes worse by scaling the technology. The keeper transistor ($M_b$) is used as a conventional solution for this problem. The disadvantage of using the keeper transistor to improve the noise margin of the circuit leads to a contention between dynamic node and the PDN. This will lead to a larger power consumption and speed degradation.

The power reduction techniques of dynamic gates proposed in literature can be generally categorized as follows:

a. Reducing the voltage swing of the dynamic node.
b. Improving performance of the keeper.
c. Restructuring and modifying the evaluation network.

* Corresponding author.
*E-mail addresses:* nasserian.mahshid@stu.um.ac.ir (M. Nasserian), kafikangi.m@gmail.com (M. Kafi-Kangi), maymandi@um.ac.ir (M. Maymandi-Nejad), moradi@eng.au.dk (F. Moradi).

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The first approach is effective since the dynamic power is proportional to the voltage swing. Therefore, reducing the voltage swing lead to power saving. The main advantage of the second approach is to reduce the contention current by using a weaker/smarter keeper circuitry. The last approach proposes new circuit topology of the PDN or footer transistor ($M_{Eval}$). Examples of the above mentioned techniques are discussed in Section 2.

In this paper we propose a new technique called Modified Charging-Scheme-based Domino (MCSD) circuit is proposed that is suitable for reducing the power dissipation of large fan-in *OR* gates.

The paper is organized as the follows. In Section 2 the state-of-the-art techniques for improving characteristics of the wide fan-in dynamic circuits are discussed. Section 3 presents the proposed circuit. A 40-bit Tag Comparator is designed in Section 4. Simulation results and discussions are provided in Section 5. Finally conclusion is drawn in Section 6.

## 2. Literature review

As mentioned above, the main power reduction techniques for dynamic circuits can be divided into three categories. In this section some of the existing works in the literature are discussed.

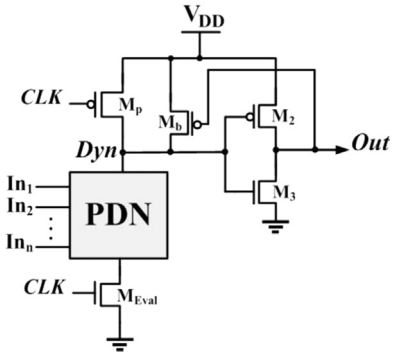


**Fig. 1.** Structure of the conventional dynamic circuit.

Generally, in the most of these approaches designers attempt to enhance one criterion (delay, power, noise margin or area) at the expense of degrading another one.

### 2.1. Single-Phase (SP) Domino

In Ref. [13] a limited switching technique called SP-Domino is proposed to realize 8-input and 16-input *OR* gates (*OR*-8 and *OR*-16). Fig. 2-a shows the SP-Domino circuit. In this technique, the dynamic node is not charged in the precharge phase. By the use of a clock signal ($CLK_i$) and its delayed version ($CLK2_i$), the keeper will charge the dynamic node to $V_{DD}$ at the beginning of the evaluation phase only if the PDN is off. As a result, the switching rate of the dynamic node is limited which results in decreasing dynamic power loss.

### 2.2. Reduced swing domino logic

Another technique to reduce the power consumption of dynamic circuits is voltage swing reduction of dynamic nodes by lowering/raising the high/low voltage values as shown in Fig. 2-b [14–17]. In this approach two voltage levels ($V_{DDL} < V_{DD}$ and $V_{GNDH} > V_{GND}$) are generated by diode-connected transistors. The voltage of the dynamic node swings between $V_{DDL}$ and $V_{GNDH}$. This leads to power saving in dynamic node due to the power consumption dependence to the voltage swing on some expanse of performance. The main drawback of this technique is the leakage current generated in the succeeding stage, when the following stage is a full swing gate. In addition, converting the low swing voltage levels to the full swing voltage levels is a non-trivial task. Moreover, if $V_{DDL}$ and $V_{GNDH}$ are generated by diode connected MOSFETs, the voltage swing will be affected by process variations.

### 2.3. Variable threshold voltage keeper

As stated before, in many dynamic circuits, a keeper is used to compensate the leakage current and avoid the dynamic node to be discharged during the evaluation phase. One of the factors that increases the power dissipation of such gates is the contention

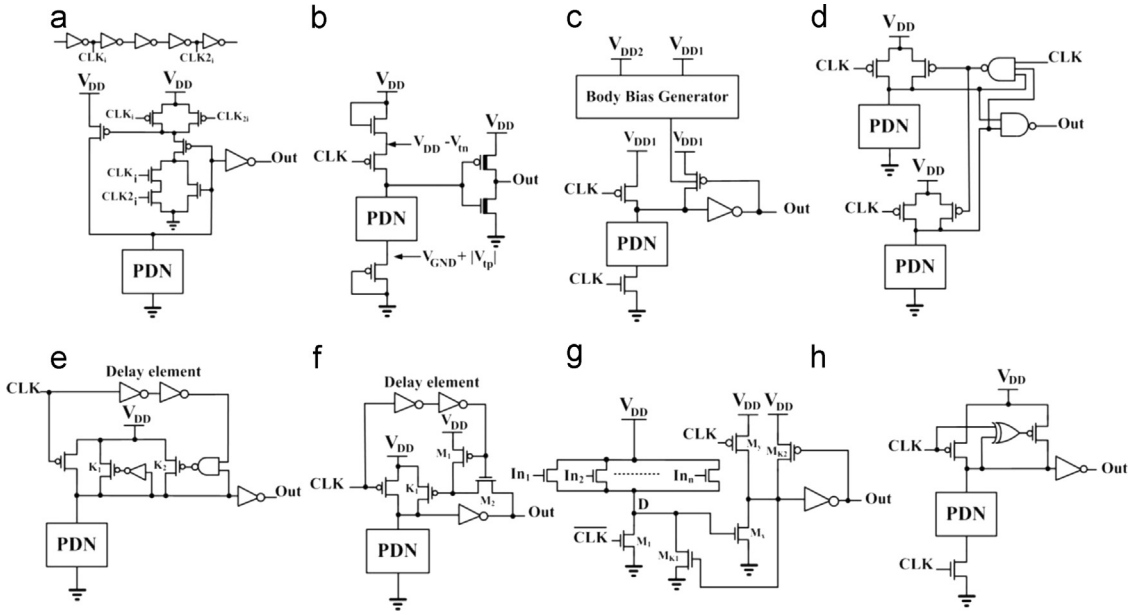


**Fig. 2.** Schematic diagram of the existing works for improving dynamic circuit characteristics by techniques: (a) Single-Phase Domino. (b) Reduced dynamic swing domino. (c) Variable threshold voltage keeper. (d) Split-Domino. (e) Conditional keeper. (f) High speed Domino. (g) SFEG. (h) Noise-tolerant XOR-based conditional keeper.