INTEGRATION, the VLSI journal 52 (2016) 168–181

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

A novel high-throughput method for table look-up based analog design automation

Yishai Statter*, Tom Chen

Department of Electrical and Computer Engineering, Colorado State University, Fort Collins, CO 80523, USA

ARTICLE INFO

Article history:
Received 11 December 2014
Received in revised form
29 July 2015
Accepted 11 September 2015
Available online 30 September 2015

Keywords:
Analog circuit design automation
Table look-up
SPICE

ABSTRACT

Analog circuit synthesis ofen requires repeated evaluations of circuit under design to reach the final design goals. Circuit simulations using SPICE can provide accurate assessment of circuit performance. Spice simulations are costly and incur significant overhead. A faster transistor-level evaluation is needed to provide higher throughput for synthesis applications. Further, miniaturization of FET's has added physical effects into SPICE models, which complicated their equations with every generation. That complication has forced analog synthesis tool developers and circuit designers alike to perform circuit evaluations using SPICE.

Analog circuit design tools largely failed in their declared goal, to take over circuit optimization tasks from human designers mainly due to over simplications using custom-developed equations for evaluating circuit performance. Since it is more and more difficult to accurately capture transistor behavior with each new generation of silicon technology, a more practical approach to analog design automation is to keep human engineers at the center of the design flow by providing them with as much needed decision-supporting data as quickly as possible. Mapping the trade-off landscape of a topology with respect to design specifications, for example, can save designers trial and error time. This approach to analog design automation requires less accuracy from the simulation sign-off tools, such as SPICE. However, it demands much faster response for circuit performance evaluations with sufficient accuracy.

In this paper, a new solution to both calculation overheads and model complexity is proposed. The proposed fast evaluation method uses a novel look-up table (LUT) algorithm to extract circuit information from complex physics-based transistor models used by SPICE. The model makes use of contemporary memory space, by replacing equations with look-up tables in addition to advanced interpolation methods. The achieved improvement is over 100 × throughput and complete decoupling from physical phenomena compared to SPICE run-time, in exchange for few gigabytes of data per device. Examples are shown for the effectiveness of replacing SPICE with our model in a transistor sizing flow, while keeping 99% of the samples inside the 5% error range on 180 nm and 40 nm CMOS processes. The proposed solution is not intended to replace sign-off quality tools, such as SPICE. Rather, it is intended to be used as a fast performance evaluator in analog design automation flows.

Published by Elsevier B.V.

1. Introduction

One of the important factors determining the success of analog circuit design automation hinges on the ability of performing repeated circuit performance evaluations rapidly and accurately. At one end of the spectrum, SPICE simulations provide the most accurate circuit evaluations, but it is too time consuming to be useful as performance evaluation tool in analog circuit design automation. SPICE simulator is widely used as a sign-off tool to determine every aspect of circuit performance and it will continue to be one of the sign-off tools. At the other end of the spectrum, equation-based compact models can be extremely fast for circuit evaluation, but they tend to be too inaccurate to be useful and hard to scale up [1,2]. This paper presents an approach of building a transistor model structure that is better suited to serve as fast circuit performance evaluation in analog circuit synthesis system.

With generational increase in technological complexity, SPICE models are also getting more complicated. The equations strategy had to be patched with a geometrical look up super layer, known as "binning". Our approach uses a novel database structure and interpolation methods to extract information from complex physics-based SPICE models to a higher level of abstraction. Therefore, the LUT approach simplifies and generalizes the model to decouple its internal structure from physical phenomena that is added to transistors' behavior with miniaturization. It also trades

* Corresponding author.

http://dx.doi.org/10.1016/j.vlsi.2015.09.003
0167-9260/Published by Elsevier B.V.

off memory for quicker queries and maximized throughput that can improve analog design automation software on a local machine and remote server.

In this paper, the results of modeling transistors from a 180 nm and a 40 nm CMOS processes are presented with the focus of capturing important parameters needed for analog circuit design automation. The transistor parameters include I_{DS}, g_m, R_o, σI_{DS}, σV_T and noise for 5 corners. The resulting models were tested for accuracy and speed compared to the results from SPICE simulations. The total storage space of the models was less than 4 GB and achieved an error standard deviation of 1.8% and access time of 1.8 μs for the slowest table.

A first application based on the proposed model to illustrate the effectiveness of the proposed approach is a transistor-sizing calculator which is referred to as "sizer" in this paper. However, the proposed approach is not intended for transistor sizing only, rather, it is intended as a fast circuit evaluation tool for analog circuit synthesis.

The sizer gets V_{DS} and I_{DS} specs and other optional constraints, such as g_m, output impedance, and noise floor etc. and calculates minimal-area transistor that meets this spec. The sizer demonstrates that the proposed model matches that of a simulator by concluding its search with a simulation and measuring the relative error between the looked-up model and the simulated one.

The implemented LUT approach has the following main characteristics:

1. GB's of look-up data
   in exchange for:
2. <2 μs queries (see Table 1. for the test setup)
3. ~2% of error stdev

2. Problem definition

Circuit synthesizers can generally be divided into two categories: generators and optimizers. Generators accept a set of performance parameters and create a set of IP library views, from netlist to layout. Their relative speed and adaptability to a range of applications could make them accepted in the industry, although they are very application and vendor-specific. Optimizers represent the opposite in approach and performance to generators. They are not provided by IP vendors, but rather remain in the realm of industry experiments and academic research. They usually need a long run time to generate a library view. They are flexible and generalized in terms of topologies and applications, but tend to be narrow on the side of library views.

A major hurdle to the usefulness and acceptance of optimizers in the industry is the long run time they require to produce a circuit. Optimizers combine abstract circuit topologies, constraints management and optimization algorithms to achieve converged solutions. Optimization algorithms typically alternate between two phases:

1. find a set of solutions and
2. Evaluate each solution according to constraints and objectives.

Table 1
Test system spec.

Resource	Value
CPU	AMD Phenom(tm) II X4 955
#Cores	4
Freq.	2.5 GHz
RAM	12 GB
OS	CentOS 6

The evaluation phase can be done with a set of equations or by a circuit simulation tool such as SPICE. The approach using equations saves significant amount of run-time, but is hard to maintain with the growing number of physical phenomena that affect transistors behavior in each technology generation. Furthermore, equations, no matter how complex they can be, have limited capability to predict accurately the performance of a given circuit. The simulation approach, though very accurate, creates a run-time bottleneck and limits the amount of performance evaluations one can perform during analog circuit optimization cycles.

The bottleneck the approach using SPICE-class simulators has three parts:

1. SPICE-type simulation is not the fastest way to evaluate a circuit. There are many overhead calculations (such as nodal analysis) that can be avoided when only a narrow set of performance parameters of some components is needed. There's also some overhead that can be saved when accuracy can be traded for speed.
2. At the implementation level, the simulator is often an external process, with all the inter-process communication overhead this entails. Alternatively, the optimizer itself is implemented as an interpreted script in the simulator's language (Tcl or Skill). Either way, there's run-time penalty to this type of modularity.
3. The long time it takes to evaluate a circuit via simulation has influence on the search itself. Search algorithms that use black-boxed simulation for evaluations try to do more guesswork to avoid too many time-consuming iterations. Therefore, the quality of search in terms of search space will be compromised leading to sub-optimal solutions.

For example, the operating-point analysis inside the BSD open-source simulator NGSpice calls the internal model equations batch 5 times per transistor, which means that even simple.op command takes ~700 μsec per transistor (on the test machine, see Table 1), on top of the unavoidable SPICE interface overhead. The time penalty paid by circuit sizing software is bound to grow with each technology generation. The "atomic" standard model is already patched and wrapped with a high level geometrical binning, which is in effect an admission of both foundries and tool-vendors that look-up techniques are more generalized and flexible than fitted equations.

The LUT based models proposed in this paper tackle the bottleneck in two different ways: high-throughput and scalability. High throughput of the models is achieved through consolidating all the parameterized physics equations into simplified look-ups and interpolations. Scalability of the models is achieved through data structures that can expand to meet the resolution needs of future technology generations.

3. Previous work

3.1. Circuit optimizers

Early work in the field of optimization-based circuit synthesis was achieved by iteratively running SPICE simulations of the circuit-under-design (CUD) using a set of design parameters and then deriving the next set of transistor sizes based on an optimization algorithm that was chosen from a library [1]. Other tools [2,3] used equations and symbolic analysis to optimize a design and then confirmed them via simulations. Though these tools are relatively fast, rapid scaling CMOS technology and increase in complexity of MOSFET behavior require frequent update of equations for the equation-based tools to maintain their accuracy. They became less useful than simulation-based ones as technology