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RF CMOS body-effect circuits

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Abstract

After a theoretical and analytical study of the body effect in MOS transistors, this paper offers two useful models of this parasitic phenomenon. Thanks to these models, a design methodology, which takes advantage of the bulk terminal, allows to turn this well-known body-effect drawback into an analog advantage, giving thus an efficient alternative to overcome the design constraints of the CMOS VLSI wireless mass market. To illustrate the approach, four RF building blocks are presented. First, a 0.9 V 10 dB gain LNA, covering a frequency range 1.8–2.4 GHz, thanks to a body-effect common mode feedback, is detailed. Secondly, a body-effect linearity controlled pre-power amplifier is presented exhibiting a 5 dB m input compression point (ICP1) variation under 1.8 V power supply for half the current consumption. Lastly, two mixers based on body-effect mixing are presented, which achieve a 10 dB conversion gain under 1.4 V for a −52 dB LO-to-RF isolation. Well suited for low-power/low-voltage applications, these circuits implemented in a 0.18 μm CMOS VLSI technology are dedicated to multi-standard architectures and system-on-chip implementations.

Keywords: LNA; Mixer; Power amplifier; CMOS; RF; VLSI; Body effect

1. Introduction

During the 1990s, the tremendous growth of the wireless mass market, led by low-cost requirements, pushed the designers to use CMOS technologies in radio frequency (RF) parts of transceivers. To achieve the highest level of system integration and also to lower the cost, RF and analog circuits must be combined with digital blocks within a single CMOS VLSI technology [1]. However, the latter, while optimized for digital rates improvement, is not well suited to handle efficient RF functions like bipolar technologies. Even if RF CMOS architectures are available to fulfill the modern telecommunication standard requirements, designers face many difficulties [2]. Among them: the set of available active and passive devices is quite limited [3]. The strong desire to keep power consumption and size of the communication devices to a minimum, combined with higher data rates, induces the shrinking of gate length. So the main drawback is still the constant λ-scaling rule, which tends to reduce drastically the supply voltage with gate length for each CMOS generation technology. Currently, in a 90 nm standard CMOS VLSI technology, nominal voltage is only 1.2 V if not lower. Under such a power supply, some regular RF topologies cannot operate, highlighting the limitations of the classical design approach.

So, is there any design solution to address this statement? The body effect through V_T control seems to be a good alternative to provide and/or improve RF circuits operating under low-power/low-voltage constraints [4].

First, studying the physical phenomenon of body effect through analytic expressions, two models are developed in Section 2 to be further used in analog circuits. Section 3 presents the contribution of body effect to improve a current reuse LNA topology with inductive degeneration. Section 4 features a body-effect linearity-controlled pre-power amplifier operating in the 900 MHz frequency range. Section 5 implements the ability of mixing operation thanks to the small-signal approach of body effect. Two mixers based on this theory are depicted. To conclude, body-effect contribution to low-power/low-voltage applications is discussed, relying on measurement results of the previously presented different RF building blocks.

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2. Body-effect analog modeling

A well-known parasitic effect of MOS transistors is the body effect. The latter is induced by a differential voltage between substrate and source and can be expressed as follows [5]:

$$V_T = V_{T0} + \gamma\sqrt{2\varphi_F}\left[\sqrt{\left(1 - \frac{V_{BS}}{2\varphi_F}\right)} - 1\right], \quad (1)$$

where V_{T0} is the intrinsic threshold voltage, γ the body-effect coefficient, $2\varphi_F$ the surface inversion potential of silicon and V_{BS} the bulk-source voltage.

Two approaches can be considered regarding expression (1), depending on the type of signal applied between bulk and substrate: dynamic or static.

First, assuming $V_{BS} \ll 2\varphi_F$ which is the "small-signal" approach, and applying Taylor series to expression (1), that leads us to

$$V_T = V_{T0} + \alpha V_{BS} \Rightarrow \alpha = -\frac{\gamma}{2\sqrt{2\varphi_F}}. \quad (2)$$

This relation (2) highlights a linear relationship between the threshold voltage of the MOS transistor and the potential applied to its bulk.

Regarding the static or DC mode, expression (1) is directly introduced in the MOS drain current expression:

$$I_d = \frac{\mu_n C_{ox} W}{2L}\left\{V_{GS} - \left[V_{T0} + \gamma\sqrt{2\varphi_F} \times \left[\sqrt{\left(1 - \frac{V_{BS}}{\sqrt{2\varphi_F}}\right)} - 1\right]\right]\right\}^2. \quad (3)$$

And so $I_D(V_{GS}, V_{SB})$ curves are plotted in Fig. 1. Fig. 1 points out that larger the V_{SB}, higher the V_T. For a given V_{GS}, I_D current flowing through the MOS transistor depends on bulk-to-source voltage. Hence, the transistor biasing can be controlled thanks to body effect in a DC approach. However, one has to pay attention to the fact that the V_{SB} range is limited. Indeed, if the V_T enhancement induces no significant parasitic constraint on DC characteristics despite the current decrease, the reduction of the threshold voltage can disturb the transistor effect. Assuming that V_{SB} is lower than roughly speaking −700 mV, the bulk-to-source PN junction of the NMOS transistor is thus forward biased, producing a leakage current and aborting the transistor functionality. It sets up the limit whose body effect is useful to implement a function thanks to the DC approach.

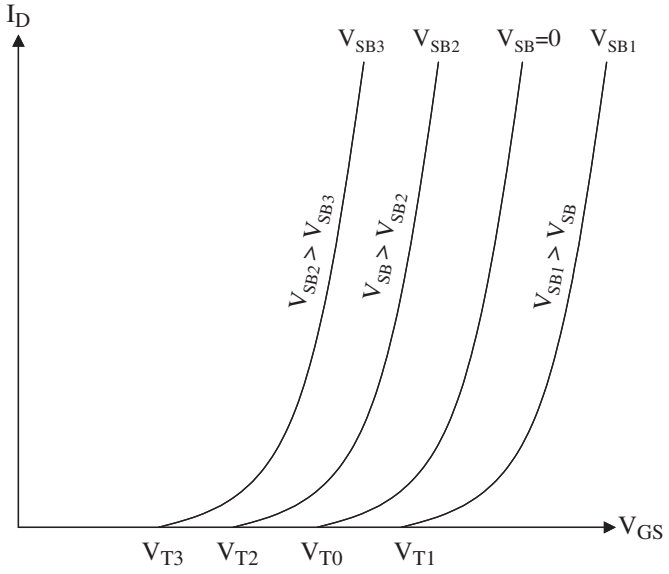

Fig. 1. I_d versus V_{GS} for different V_{SB}.

Now, we are going to present different circuits using the body effect to provide or improve RF functions under low supply voltage. Also, keeping in mind the low-cost constraint induced by mass market, a PMOS transistor is always used to perform the body-effect operation in the following circuits so as to be VLSI compatible. It would thus avoid the use of expensive triple-well technologies. However, triple well becoming a kind of standard in deep submicron technologies, we can derive at this time the same design approach to NMOS in such a case and then benefit from their better frequency ability versus PMOS counterparts.

3. Body-effect biasing control in LNA

A key building block for the RF front end is the low-noise amplifier (LNA), which precedes a high-noise stage (e.g. image-reject filters or mixers), and plays a critical role in determining the overall noise figure (NF) of a given receiver. Friis analytic expression demonstrates that the higher the conversion gain (S_{21}), the lower the NF [6].

Under low-voltage constraints, the output voltage swing, and so the gain, are dramatically reduced, which limits the overall NF optimization. The useful cascode topology [7], stacking two transistors between supply rails, then limiting output head room voltage, is directly concerned by this drawback. To overcome this kind of problem, a reuse inductive degeneration (RID) topology [8] was implemented as depicted in Fig. 2.

(L_{G1}, C_{GSMP}, L_{S1}) and (L_{G2}, C_{GSMN}, L_{S2}) appear as two parallel input paths of a cascade structure i.e. the inductive degeneration topology. Each one is matched to 100 Ω so as to provide the overall 50 Ω input impedance, when M_N and M_P are connected together in a current reuse topology. Thus, this active load concept of reuse architecture also allows to reach high gain under low voltage.

Measurements presented in Fig. 3 highlight an 11 dB gain while consuming 3.8 mA under 1 V at 2 GHz, so the RID circuit of Fig. 2 meets successfully the low-power and low-voltage requirements. Nevertheless, achieving a 1.8 dB NF and a 650 MHz bandwidth, the circuit does not perfectly fit with theoretical expressions of a classical inductive degeneration gain-NF optimization. It can be explained by the common mode feedback (CMFB) loop