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Low power dynamic logic circuit design using a pseudo dynamic buffer

Fang Tang*, Amine Bermak, Zhouye Gu

The Hong Kong University of Science and Technology, ECE Department, Clear Water Bay, Kowloon, Hong Kong

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ABSTRACT

In this paper, we propose a pseudo dynamic buffer (PDB) for footed domino logic circuit implementation. Using the proposed PDB structure, the output pulse during the precharge process is prevented from propagating to the output stage, as is the case in conventional case. As a result, up to half of the power is saved compared to a conventional domino gate, while improving the sampling window of the dynamic gate. This PDB structure is applicable not only for Pull-down network (N-type) dynamic logic, but also for Pull-up networks (P-type). Simulation results illustrate improved performance using the proposed scheme compared to the conventional dynamic logic for different loading conditions, clock frequencies and logic functions. In addition, our proposed design reduces the clock loading from conventional three to two transistors. As a result, the proposed scheme significantly saves power due to lower load capacitance on the clock bus. Test structures are fabricated in 0.35 μm CMOS technology. Measurement results validate the proposed concept and illustrate power saving as compared to conventional design.

1. Introduction

Dynamic logic has been very widely used in a large number of applications such as high speed digital logic [1–3]; memory [4–6] as well as high performance microprocessor design [7,8]. This logic family offers a number of interesting features compared to static logic, namely reduced transistor count (almost half compared to static complementary) as well as reduced load capacitance and hence improved speed. The operation of a dynamic logic gate is controlled by a clock signal and can be implemented in either Pull-up (P-type) or Pull-down (N-type) configurations [9]. The voltage at the output of the dynamic circuit is stored on a parasitic capacitance, which is typically buffered before it is sent to the next stage. This temporary voltage is affected not only by charge sharing of the internal parasitic capacitances [10], but also by the consequent dynamic circuit. Normally, a buffer at the output of the dynamic logic is required to drive the next stage. A typical domino gate [9] consists of a P-type or N-type network followed by a static inverter. In general, a Keeper (or bleeder) is added in order to alleviate charge sharing problems [11]. Since the output of the dynamic gate is sampled on parasitic capacitances, periodic precharge phases of the output node are required. Although dynamic logic circuit benefits from smaller area and higher speed, a significant power is waisted due to these periodic precharge phases. Additionally, these precharge pulses introduce extra noise in the gate and the propagation of these pulses through the static buffer result in extra power consumption [12]. TSPC-based dynamic logic circuit proposed in [13] can significantly reduce the propagated noise, since the buffer is disabled during the precharge phase by an extra stacked clock transistor. However, this additional clock transistor increases the load capacitance of the clock signal and eventually, extra power is consumed due to larger clock loading. In this paper, we propose a pseudo dynamic buffer (PDB) for the footed clock controlled dynamic logic circuit. Using this PDB structure, the precharge pulse is blocked at the input of the buffer and is prevented from being propagated to the output of the dynamic gate. As a consequence, power typically consumed in the buffer during the precharge phase is saved. Additionally, compared to TSPC-based dynamic logic, in our scheme the clock transistor count is reduced from 3 to 2. As a result, the power consumption of our proposed scheme is significantly reduced due to lower load capacitance on the clock bus.

This paper is organized as follows. In Section 2, the conventional domino logic gate is reviewed and the proposed dynamic logic gate based on the pseudo dynamic buffer is introduced. Section 3 introduces a thorough performance analysis of the proposed gate in terms of power consumption as well as cascading and charge sharing properties. Section 4 introduces simulation and experimental results of the proposed logic structure. Section 4 also provides performance comparison of the proposed dynamic gate against the conventional structure for different logic gates and under different loading and frequency assumptions. Comparison results are based on both simulation as well as

* Corresponding author.
E-mail address: bermak@ieee.org (F. Tang).

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experimental measurements from the fabricated test structures. Section 5 presents a conclusion.

2. PDB-based domino logic

2.1. Conventional domino logic

Fig. 1A shows the schematic of a conventional footed clock controlled domino logic circuit, which consists of a dynamic N-type gate (Pull-down network PDN) followed by a static inverter. Fig. 1B illustrates the implementation of a domino logic buffer. The gate operates in two phases, namely precharge and evaluation phases. During the precharge phase the clock signal *clk* is pulled low thus turning on the PMOS transistor *M*1 enabling to precharge the dynamic node *Z*. During the evaluation phase, the clock signal *clk* is pulsed high, thus turning on the NMOS transistor *M*2. When the input A is low, the logic at node *Z* is kept high regardless of the operating phase. However, when the input *A* is high, two phases (evaluation and precharge) should be discussed as depicted in Fig. 2. During the precharge phase, node *Z* is charged up to *V*dd as well as node *B*. The voltage at node *F* drops down to '0', resulting in a propagation of the precharge phase to the output of the buffer.

The propagation of the precharge pulse from node *Z* through the static buffer results in increased power consumption. In addition, the output logic is unstable during the precharge phase

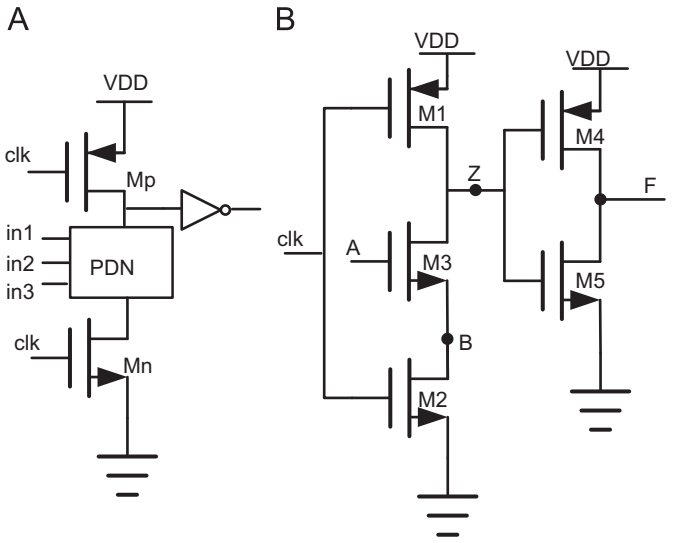

Fig. 1. (A) A typical domino logic circuit using the conventional buffer. The buffer is a static inverter, which connects the source of *M*5 to *Gnd*. (B) Domino buffer implementation example.

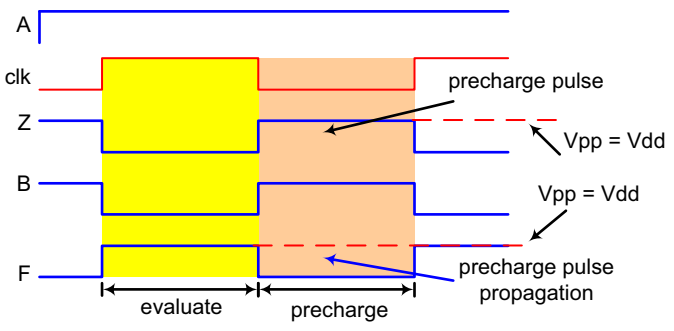

Fig. 2. Timing diagram of the conventional domino logic circuit, when input logic *A* is '1'. Note that the precharge pulse is propagated through the buffer.

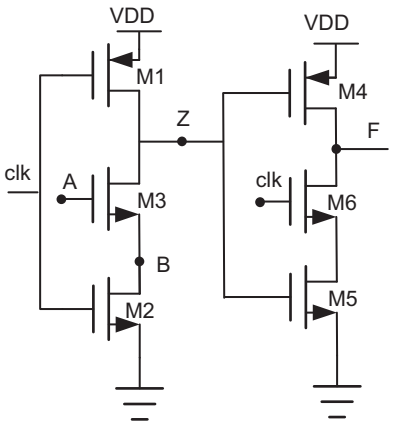

Fig. 3. TSPC dynamic logic circuit using NC^2MOS output buffer. The output node *F* holds its previous value and is isolated from the precharge pulse at node *Z* during the precharge phase.

and as a result the cascading performance is limited [8]. A number of solutions were proposed to deal with this issue of precharge pulse propagation [12,13]. Amongst other solutions, the TPSC dynamic logic scheme proposed by Ji-Ren et al. [13] overcomes such a problem using NC^2MOS or PC^2MOS, as shown in Fig. 3, but at the expense of an extra transistor as compared to a domino gate. In this gate, the dynamic node *Z* is precharged high and *M*6 is disabled. As a result, the output *F* holds its previous value [13]. However, the TSPC design suffers from the drawback of doubling the load capacitance for the clock signal, which results in increased power induced in the clock distribution network. This power constitutes a very significant component in modern digital processor design [14]. Large clock loading will cause a slow clock edge and therefore, extra power is consumed when transistors *M*1 and *M*2 are turned on at the same time leading to an increase in short circuit current during the clock signal transition.

2.2. Proposed PDB for domino logic

The previous section illustrates the issue of performance degradation due to the propagation of the precharge pulse inherent in domino logic gates. The proposed PDB-based implementation overcomes this problem using the circuit structure shown in Fig. 4. In the proposed implementation of the buffer, the source of the buffer's NMOS transistor *M*5 is connected to node *B* instead of *Gnd*. Using such a circuit topology, the value at node *Z* cannot propagate to the output *F* during the precharge phase of the gate since during this phase, the evaluation transistor *M*2 is turned off. For our proposed gate, when the input logic *A* is low, the floating node *Z* is always high and then, the output node *F* is kept low regardless of the operating phase. On the other hand, if the input *A* is high, the precharge and evaluation phases will lead to the following situation:

- During the evaluation phase, node *Z* is discharged to *Gnd* as well as node *B*, resulting in enabling the PMOS transistor *M*4, while pulling up the output *F* to Vdd.
- During the precharge phase, node *Z* is charged up to *Vdd*, followed by the voltage at node *B*. Since the NMOS evaluation transistor *M*2 is disabled, the output node *Z* is held high (same value as the previous evaluation phase).

The timing diagram of the proposed circuit for the case when the input *A* is high is illustrated in Fig. 5. It is also worth mentioning that a voltage drop at node *F* is assumed with an amplitude of Vpp' (ideally $Vpp' = 0$). It is important to note that