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Self-aligned electron beam lithography of metallic layer sandwiched in a polymer multilayer: Facilitation of vertical organic transistor fabrication

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ABSTRACT

Electron beam lithography in multilayer of resist including an intermediate metallic layer is proposed for fabrication of novel three dimensional structures. The feasibility of the proposed process and the possible line width resolution has been analyzed. A Self-aligned vertical stack of polymer with an intermediate metallic layer has been achieved using the technique. The three dimensional pattern has been shown to facilitate fabrication of vertical organic transistor. A vertical organic transistor with poly(3-hexylthiophene) as active material is fabricated. The transistor shows high current output at low operating voltage. The direct write technique consists of minimum number of steps and is capable of providing well defined gate geometry for the transistor in contrast with other non-lithographic techniques.

1. Introduction

Though electron beam (EBL) lithography is primarily used for its advantage of having better resolution (sub 10 nm) than optical methods, there is another crucial difference which sets it apart from optical lithography [1–6]. The performance of optical lithography strongly depends on the optical absorption properties of the resist materials. Electron beam, on the other hand being energetic charged particles, interacts with the resist material via coulomb interaction irrespective of their optical properties leading to distinct nature of energy deposition profile of its own [1]. This makes electron beam lithography applicable for patterning of three-dimensional structures in multiple layers of resists in a single exposure. Thus far use of EBL in multiple layers [7–11] of resist for three-dimensional patterning has been limited to layers of polymer resists of different sensitivity and the electron energy deposition through the soft polymer resist materials are almost uniform. In many applications a device designer seeks to incorporate a layer of metal in a stack which need be patterned along with the multilayer stack. A multiple exposure sequential process of achieving this through standard lithography is not a viable technique. Further metallic layer being an attenuating medium for optical radiation cannot be used for through exposure. In EBL though, inclusion of an intermediate metal layer would alter the electron energy deposition profile (latent image) through these multilayers. We propose e-beam patterning of such multilayer in single exposure, which may allow for obtaining automatic alignment of the latent image written on the top and the bottom resist layer including a metallic grid. E-beam exposure, followed by development/etching would result in micro-patterned self-aligned vertical stack including the metallic layer. In this paper we report the energy deposition profile of 30 keV electrons in a multilayer resist stack which consists of an aluminium layer sandwiched between widely used positive tone electron beam resist PMMA and discuss the implications of the metallic layer on the energy deposition profile which is closely related to the viability of EBL in the multilayer. The line width resolution of EBL in such multilayer is also reported. As a test-case application of EBL in such multilayer, we demonstrate facilitation of fabrication of the buried metal grid of a vertical organic transistor based on poly(3-hexylthiophene) (P3HT) which is a polymer semiconductor.

The vertical organic transistor has attracted attention of the researchers in organic electronics due to their low operation voltage and high output current characteristics owing to their short channel length which is realized by exploiting the thickness of the semiconductor as the channel length [12–16]. In most of the vertical transistor an intermediate gate electrode is inserted in the middle layer of the vertical stack of the source/semiconductor/drain [14–16]. The potential applied to the gate controls the current between the source and the drain. To allow the carrier flow across the gate it is required to be patterned to have openings. The patterning of the intermediate gate layer is an important process

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step in defining the device structure since it controls the device operation mechanism and performance. Watanabe et al. has used shadow mask technique to deposit micron spaced parallel aluminum film strips buried in semiconductor layer [16]. In this technique the active material is deposited in two stages, moreover an insulating layer on both the sides of the gate layer is required to reduce the gate leakage current [17]. Chao et al. has used a non-lithographic technique using self-assembled polystyrene spheres as shadow mask to achieve submicron pores on the intermediate aluminum gate layer, subsequently they used oxygen plasma etching to form deep vertical pores in PVP dielectric layer below the patterned aluminum layer [15]. The device resembles the solid state version of a triode in which organic semiconductor is filled in the numerous vertical columns and the space charge limited current through the columns are controlled by the potential at the intermediate aluminum grid. However the fabrication process involves controlled plasma etching and an additional step devoted for the insulation of the upper surface of the Al gate layer is necessary to reduce the gate leakage current [18,19]. We show that a self-aligned vertical stack including a metallic layer patterned using EBL on a multilayer resist stack as proposed earlier, readily provides the template needed for a vertical transistor with an intermediate gate layer insulated from both sides. The fabrication process consists of minimum number of steps, and well-defined grid geometry is easily achieved. A complete understanding of the functioning principle of vertical transistors using organic semiconductors is yet to emerge, and experimental data on varied device geometry will help in understanding and controlling of the underlying mechanisms better. The direct write technique described here will allow rapid prototyping of devices with varied device geometry. Even though its application for large scale fabrication is not envisaged at this stage of development of vertical organic transistor (VOT), the models so developed will of help in establishing the required control in resolution and performance of the grid.

In the following section we present the electron energy deposition profile inside the multilayer and discuss the effect of the metal layer on EBL in such multilayer. The details of the vertical organic transistor fabrication and the device characterization and discussion are followed next.

2. Electron energy deposition profile in the multilayer

The fundamental step in the process of electron beam lithography is the energy deposition by the electrons inside the resist film during the e-beam scanning. The energy deposition selectively modifies the resist and the pattern is formed during the subsequent development, thus uniform spatial energy deposition over the region desired to be developed is essential for EBL. In a multilayer resist with an intermediate metal layer the rate of electron energy loss as well as the elastic scattering will be higher at the metallic layer as both of them increase with target density and atomic number [20]. Thus it would be important to analyze the spatial energy deposition profile of keV electrons typically used in EBL for a multilayer resist stack which includes a thin metal layer. More specifically, the effect of electron scattering and energy loss in the metallic layer on the resolution of the electron beam lithography in the tri-layer.

We have obtained the spatial energy deposition profile and line width resolution for 30 keV electron beam lithography in a tri-layer film of PMMA (70 nm)/Al (40 nm)/PMMA (60 nm) over a 140 nm thick ITO coated Glass substrate. A similar tri-layer film/substrate is used in a device fabrication in the following section. The spatial distribution of electron energy on a single layer PMMA film of equal thickness (170 nm) on the ITO/Glass substrate is also obtained to distinguish the effects of the metallic layer. The spatial energy deposition data was obtained by using the Monte Carlo simulation software CASINO [21,22]. Fig. 1(a) and (b) show the spatial energy deposition density profile for line scans with a 30 keV electron beam of diameter 2 nm over the tri-layer and a single layer film/substrate. The profiles show the cross-sectional view of the energy deposition density in units of eV/cm^2/electron for line exposures. Comparing Fig. 1(a) and (b) one can see that the spatial broadening of the equienergy contours increases only by 3 nm in the bottom PMMA layer of the tri-layer film. This indicates that beam broadening due to elastic scattering at the metal layer is very low and the achievable resolution of electron beam lithography in the tri-layer would be almost same as that of single layer resist film. The mean free path of electrons between elastic scattering by the target atoms of a medium is given by $\lambda = A/N_A\rho\sigma_e$, where A is the atomic weight, N_A is the Avogadro's number, ρ is the density of the medium and σ_e is the total elastic scattering cross section [20]. The kinetic energy lost by the electrons in traversing through the top PMMA resist layer is negligible and to a fair approximation we can assume that the energy of the electrons are still 30 keV when they enter the Al layer. Thus we calculate the mean free path of 30 keV electrons in the Al target which turns out to be 38.3 nm. The thickness of the Al layer is 40 nm which indicates that most of the electrons escape the Al metal layer without suffering an elastic collision. However the electrons will lose energy inside the aluminum layer with an increased rate. If a higher energy e-beam is used the mean free path will be longer and scattering will go down further. One may note that the thickness of the Al layer used in this analysis is suitable for many applications. The energy deposition density distribution in units of eV/cm^3 can be found by multiplying the contour values in Fig. 1(a) and (b) by the dose of line exposure (electrons/cm). The line width after development for a particular line exposure dose can be predicted by identifying the equienergy deposition density (eV/cm^3) contour corresponding to the threshold exposure energy density. The threshold exposure energy density for a particular resist and developer solution is the energy density above which the resist becomes soluble in the developer solution. The threshold exposure energy density for PMMA is 1×10^{22} eV/cm^3 for MIBK/IPA (1:3) developer solution [23]. If we multiply the contour values in Fig. 1(a) and (b) with a line exposure dose 1.6×10^{-8} C/cm (typical for PMMA), the contour of 0.5 ($\times 2 \times 10^{11}$ eV/cm^2/e) corresponds to the energy deposition density 1×10^{22} eV/cm^3. This indicates that the achievable line width would be 24 and 30 nm in the single layer and the tri-layer film respectively. Thus we can see that self-aligned patterning through the tri-layer film is possible with 30 keV electron beam and the achievable resolution would be same as that of single layer resist.

3. Materials and methods for VOT fabrication

3.1. Device structure

The schematic of the vertical organic transistor is shown in Fig. 2. The device consists of an array of vertical columns of P3HT filled in cylindrical pores perforated in the vertical stack of PMMA/Al/PMMA. PMMA is a standard electron beam resist and a dielectric material as well. The buried Al layer with array of circular opening on it acts as the grid. Holes are injected from the top Au electrode into the P3HT layer and get collected by the bottom ITO electrode. Space charge limited current flows through the vertical columns of P3HT and the current along the length of the columns is controlled by the potential applied to the Al grid. The diameter of the circular opening is 5 μm and they form a square array with centre to centre distance 15 μm. The array spans across 800×800 μm^2 area. When positive potential is applied to the gate,