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Double gate dielectric stacks with Gd_2O_3 layer for application in NVSM devices

Robert Mroczyński [a,*], Jakub Jasiński [a], Heinrich Gottlob [b], Matthias Schmidt [b]

[a] Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Koszykowa 75, 00-662 Warsaw, Poland
[b] AMO GmbH, Otto-Blumenthal-Strasse 25, 52074 Aachen, Germany

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ABSTRACT

This work presents the feasibility study of application of gadolinium trioxide (Gd_2O_3) layers in double-gate dielectrics stacks for non-volatile semiconductor memories (NVSM). In the course of this work metal–insulator–semiconductors (MIS) structures with SiO_2/Gd_2O_3 stacks have been fabricated and characterised by means of current–voltage (*I–V*) and split-*CV* techniques. Moreover, memory characteristics were investigated and compared to MIS structures with stacks based on atomic layer deposited (ALD) hafnium dioxide (HfO_2) and aluminum trioxide (Al_2O_3) layers. Presented results have shown low leakage current density of fabricated SiO_2/Gd_2O_3 of the order of 10^{-6} A/cm^2 at 5 MV/cm of equivalent electric field intensity, low interface trap density (N_{it}) $\sim 2 \times 10^{11}$ cm^{-2} and moderate mobility of MISFETs with studied stacks in the range of 140–380 cm^2 V^{-1} s^{-1}. Moreover, the decrease of retention time extrapolated at ten years of the order of 12% was determined which is significantly lower in comparison to MIS stacks with ALD high-*k* dielectric layers. In the case of MISFET's threshold voltage (U_t) relatively broad memory window has been obtained around 1.67 V which makes the investigated double-gate dielectric stack as the potential candidate for low voltage memory applications.

1. Introduction

Due to scaling issues there is no doubt that future generations of non-volatile semiconductor memories (NVSM) will be based on high permittivity (high-*k*) dielectric materials [1,2]. Nowadays, the key technologies for the NVSM devices fabrication are floating gate flash (FG) and silicon–oxide–nitride–oxide–silicon (SONOS) [3]. However, charge-trapping type memories based on dielectric materials are easier to integrate into high volume manufacturing, also due to the better scalability. As a consequence, extensive studies towards the application of high-*k* dielectric layers into the gate stack of metal–insulator–semiconductor field effect transistor (MISFET) are being performed. There are many examples of papers that have already shown the feasibility of application of alternative dielectrics, i.e.: hafnium oxide (HfO_2) [4], hafnium oxynitride (HfO_xN_y) [5], zirconium oxide (ZrO_2) [6] and lanthanum-based dielectrics (LaO_x) [7] in MOSFETS for memory applications. Furthermore, after announcement that the FinFET will be a core transistor architecture in the 22 nm generation node [8], initial studies concerning the fabrication of FinFETs for NVSM applications with classical silicon dioxide (SiO_2), as well as hafnium dioxide gate dielectric layer were also demonstrated [9,10]. However, among rare earth oxides, gadolinium trioxide (Gd_2O_3) with its relatively high permittivity value ~16 was proven recently as thermally stable in the gate first process integration scheme which makes him also a possible candidate as a replacement MOSFET gate insulator [11].

In this work we present the feasibility of application SiO_2/Gd_2O_3 stack in NVSM devices. The results reported in our recent work [12] have proven that a gate stack which is composed, in contrary to commonly found in the literature, of only two gate dielectric layers, demonstrates a great hope of application in NVSM devices. The quality of double gate dielectric stack was investigated by means of split-capacitance–voltage (split-*CV*) and current–voltage (*I–V*) characteristics analysis. Memory characteristics were assessed by monitoring the shift of threshold voltage (U_t) of MISFET upon the program and erase operations, which corresponds to program/erase voltage values ($U_{p/e}$), at elevated temperatures (up to 85 °C). Moreover, the comparison with previously reported results [13] with atomic layer deposited (ALD) high-*k* layers was performed.

2. Experimental

2.1. MISFETs preparation

N-channel MISFETs have been fabricated on <100> bulk silicon (resistivity of 15–25 Ω cm) using a specially developed gate first integration approach at the advanced microelectronic center aa-

* Corresponding author. Tel.: +48 22 234 6065; fax: +48 22 234 6063.
E-mail address: rmroczyn@elka.pw.edu.pl (R. Mroczyński).

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chen (AMICA), AMO GmbH (Germany). In order to remove organic and metallic residual contaminants silicon wafers were cleaned prior the processing within standard radio corporation of America (RCA) cleaning solutions. After RCA cleaning, substrates were fully rinsed and immersed within high-purity DI (deionised water). Immediately after cleaning process silicon substrates were introduced into thermal processing to start double gate dielectric stack fabrication. At first, 4 nm SiO_2 layer was obtained by thermal oxidation of silicon followed by 10 nm Gd_2O_3 e-beam evaporation [14,15]. For gate electrode, a mid-gap titanium nitride (TiN) obtained by reactive magnetron sputtering in nitrogen ambient from a Ti target metal inserted poly-silicon stack (MIPS) has been used. Arsenic dopants for source and drain have been activated by rapid thermal annealing (RTA) process at 930 °C after self aligned ion implantation.

2.2. MIS capacitors with ALD high-k dielectric layers fabrication

In the course of this work the comparison to previously reported results obtained for double-gate dielectric structures with ALD dielectric layers have been performed. However, in order to perform fairly and quantitative comparison additional metal–insulator–semiconductor (MIS) capacitors with double-gate dielectric stacks were fabricated. Those structures were composed of silicon oxynitride (SiO_xN_y) and silicon dioxide as the pedestal (bottom) dielectric layers and hafnium dioxide and aluminum trioxide (Al_2O_3) as the top dielectric.

PlasmaLab Oxford system 80+ and standard high temperature furnace were used to fabricate ultra-thin (~5 nm) silicon oxynitride at 350 °C and silicon dioxide pedestal layers at 900 °C, respectively, on 2-inch silicon <100> "p" substrates (6–10 Ω cm resistivity) cleaned just prior to the processing by RCA method.

Hafnium dioxide and aluminum trioxide high-*k* top dielectric layers were deposited by ALD method in a Savannah-100 reactor from Cambridge NanoTech Company. DI water as an oxygen precursor, tetrakis (dimethylamido) hafnium (TDMAH) as a hafnium precursor and trimethylaluminum (TMA) as an aluminum precursor were used. Two types of MIS structures were fabricated: with the physical thickness of both dielectric layers 10 and 15 nm. A Horiba Jobin–Yvon ellipsometer allowing measurements at different angles of incidence with the wavelength ranging from 190 to 850 nm was used to determine the thickness of examined layers. Growth temperature turned out to be the most important parameter in the ALD process. More details about optimisation of high-*k* ALD process can be found elsewhere [16]. Dielectric layers were obtained at 85 and 200 °C, in case of hafnia and alumina, respectively, by double-exchange chemical reactions:

- $Hf[(CH_3)_2N]_4 + 2H_2O \rightarrow HfO_2 + 4HN(CH_3)_2$,
- $2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$.

Vacuum evaporated aluminum was used as the metal gate, which completed gate stack of MIS structures, fabricated using non-self-aligned technology.

2.3. Electrical characterisation

The electrical measurements were performed with the Keithley 4200 semiconductor characterisation system equipped with SUSS PM-8 Probe Station which allows for electrical measurements at elevated temperatures (in the range of −60 to +200 °C). The MISFETs with various channel length were used allowing the determination of basic electro-physical properties of the investigated SiO_2/Gd_2O_3 stacks and structures. In the case of ALD layers MIS capacitors with gate area $A = 1.9 \times 10^{-5}$ cm^2 were used allowing the determination of electrical parameters.

3. Results and discussion

3.1. Electrical characterisation of MISFETs with SiO_2/Gd_2O_3 stack

Basic electro-physical parameters of obtained MISFET devices have been evaluated. The equivalent oxide thickness (EOT) value of gate dielectric stack ~5 nm was determined based on the maximum value of capacitance (C_{MAX}) in the accumulation direction. The EOTs of investigated in this work double-gate dielectric stacks have been evaluated based on the maximum capacitance of MIS structure in the accumulation regime. We have used following equation:

$$\mathrm{EOT} = \frac{\varepsilon_0 \varepsilon_{SiO_2} A}{C_{MAX}} \tag{1}$$

where C_{MAX} was obtained by using two-point method of Majkusiak et al. [17]:

$$C_{MAX} = \left(\frac{C_1 + C_2}{2} + \frac{kT}{q}\left|\frac{C_2 - C_1}{U_{G2} - C_{G1}}\right|\right) + \sqrt{\left(\frac{C_1 + C_2}{2} + \frac{kT}{q}\left|\frac{C_2 - C_1}{U_{G2} - C_{G1}}\right|\right)^2 - C_1 C_2} \tag{2}$$

where A is a gate area, kT/q = 0.0258 V and C_1, C_2, U_{G1}, U_{G2} are coordinates of two points selected in the accumulation regime of *C–V* characteristics of MIS structure.

According to International technology roadmap for semiconductors (ITRS) this fulfils nowadays demands of structures for memory applications very well. The analysis of *J–E* characteristics of SiO_2/Gd_2O_3 stacks proved a low leakage current ~1 μA @5 MV/cm in the accumulation direction at a comparable level to a very good quality double-gate dielectric structure based on ALD HfO_2 film with similar physical thickness, but higher EOTs. The appropriate comparison is presented in Fig. 1. There were also depicted leakage current densities of other studied in this work double-gate dielectric stacks. It has to be underlined that presented leakage current densities are normalised to the equivalent electric field intensity which, in turn, were obtained based on the EOT of particular double-gate dielectric stack.

Mobility values obtained for MISFETs with double-gate dielectric stacks based on gadolinium trioxide layers have been extracted by using split-*CV* technique. By the analysis of those curves several electro-physical parameters can be evaluated. Exemplary split-*CV* curves necessary for determination of inversion charge (Q_{inv}) and depletion charge (Q_b) are presented in Fig. 2. The parasitic capacitance of the gate pad (C_{par}) was eliminated by using the procedure presented by Lime [18]. In Fig. 3, in turn, there has been depicted

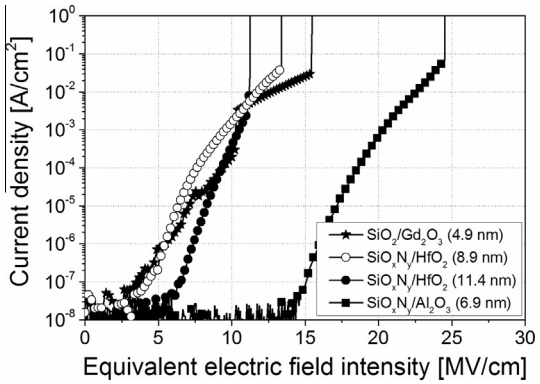

Fig. 1. Comparison of current density versus equivalent electric field intensity of MIS capacitors with different double-gate dielectric stacks; particular EOT values were taken into evaluation.