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A low-power switched-current CDMA matched filter employing MOS linear matching cell with on-chip A/D converter

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ABSTRACT

A low-power switched-current matched filter (MF) for code-division multiple-access (CDMA) systems has been developed. The front-end voltage-to-current (V/I) converter has been eliminated by merging the function into each matching cell utilizing the MOS linear I–V characteristics. A low-power analog-to-digital (A/D) converter has also been developed to establish smooth interfacing to digital back-end processing for a delayed locked loop (DLL) and a RAKE receiver. A proof-of-concept chip was fabricated in a 0.35-μm standard CMOS technology with a measured power consumption of 1.65 mW at 11 Mchip/s with 2-V power supply including the A/D converter.

1. Introduction

The direct-sequence code-division multiple-access (DS-CDMA) has been widely used in mobile applications such as cellular phones [1], wireless local area networks (WLAN) [2], global positioning systems (GPS) [3], and so forth. In DS-CDMA systems, a matched filter (MF) is an essential component. In an MF, synchronization is carried out between a base station and mobile terminals by taking correlation between the received signal and a pseudo-random noise (PN) code sequence. A number of MFs based on CMOS technologies have been developed using digital circuits [4–10] and analog circuits [11–29]. Although MFs using charge-coupled devices (CCD) [30,31] or surface acoustic wave (SAW) technologies [32–34] are also possible solutions, they are not compatible with single-chip integration. In digital implementation [4–10], although low cost and flexible system design is permitted, large power consumption is critical because a high-speed and high-accuracy analog-to-digital (A/D) converter as in [35] is indispensable at the front-end. In this point of view, analog MFs have been developed using either voltage-mode [11–21], current-mode [22–28], or charge-domain [29] circuitries aiming at low-power systems and area-efficient integration.

In terms of simple implementation, current-mode circuits are preferred because summation and subtraction operations are easily achieved using the Kirchhoff's current law. In particular, the current-mode approach is profitable due to a large number of additions and subtractions in MFs. In addition, they are feasible in deep sub-micron technologies: voltage-mode circuits would suffer from the limited dynamic voltage range as the voltage supply is lowered by scaling. In this regard, a simple switched-current MF has been developed [18] and a direct-current-cut technique has been introduced to the same type of MF for power reduction [23]. Nevertheless, the 128-chip MF fabricated in a 0.8-μm technology was estimated to consume 13.7 mA (e.g., 27.4 mW@2 V) at 4 Mchip/s operation. It is quite large as compared to the voltage-mode MFs [11–21]. This is because the substantial power dissipation occurs in the front-end voltage-to-current (V/I) converter. In order to reduce the power dissipation, a sub-block architecture was presented in [24,28], where a low-power V/I converter is provided to each small sub-block and only one V/I converter is activated at one time. As a result, the power dissipation of 1.95 mW at 8 Mchips/s has been achieved in [24,28]. In [25,26], programmable finite-impulse response (FIR) filters that can be used as MFs were proposed separately. However, chip area and power dissipation were not very small as compared to dedicatedly designed MFs.

The purpose of the present work is to develop a current-mode MF [36] which does not require a front-end V/I converter for further power reduction as compared to [24,28]. For this purpose, the V/I converter function is merged into each matching cell utilizing the MOS linear I–V characteristics in the triode region. For a good linearity, a gain-boosting technique has been

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introduced to stabilize the drain voltage of the MOS transistors for *V*/*I* conversion. In addition, in order to establish smooth interfacing with the back-end digital processors such as a delay locked loop (DLL) or a RAKE receiver, a low-power A/D converter has been developed. As a result, such a low-power operation as 1.65 mW at 11 Mchips/s has been achieved even including the power consumption in the A/D converter. The results were obtained from the proof-of-concept chip which was designed and fabricated in a 0.35-μm standard CMOS technology.

The remainder of this paper is organized as follows. The system organization is presented in Section 2. In Section 3, the building block circuits are described. The measurement results from the fabricated chip are presented in Section 4. Then the concluding remarks are given in Section 5.

2. System organization

Simplified block diagrams of conventional CDMA systems and the system we are proposing in this paper are shown in Fig. 1. The input data is firstly modulated by a modulator such as a binary phase shift keying (BPSK) modulator or a quadrature phase shift keying (QPSK) modulator and spread over a wide bandwidth by multiplying a *PN* code sequence. Then, the modulated signal is up-converted to a radio frequency (RF) signal and transmitted to receivers.

At the receiver side, after RF demodulation and quadrature demodulation, the analog baseband signal is converted to digital signal in the conventional CDMA systems (Fig. 1(a)). Then, the data are de-spread in an MF in digital domain to search for the synchronization timing between a base station and the receiver. After establishing the synchronization, the data are recovered by using a DLL and a RAKE receiver. DLL is a baseband signal demodulator composed of a discrete-time integration circuit called a sliding correlator [37]. The integration is triggered by the detected peaks in the MF. The RAKE receiver is a maximal ratio combining (MRC) receiver to combine the energies of distinct multi-path signals obtained from the DLLs [38,39]. In this manner, the signal-to-noise (S/N) ratio of the reconstructed data is improved. In this configuration, 8-bit or higher-resolution A/D conversion is required [5,30] to precisely demodulate the received signal containing the data from multiple users and multi-path fading noises. In addition, as the correlation length becomes longer and the number of multiple users becomes larger, both resolution and operational speed required for A/D conversion increase. Therefore, such high-resolution and high-speed A/D converters consume a lot of power, severely limiting the battery life of mobile terminals.

In the system we are proposing in this paper (Fig. 1(b)), on the contrary, the analog MF is equipped with A/D converters at the back-end. The function of an MF is to detect peaks in the correlation values for the synchronization and to calculate the correlation power for the RAKE receiver in the following stage. Therefore, only moderate accuracy is required for A/D conversion of the correlation values. Namely, such a system configuration as the analog CMOS MF in conjunction with the A/D conversion interface at the back-end would allow a power-efficient system implementation.

3. Building block circuits

3.1. Block diagram

The block diagram of the MF developed in this work is shown in Fig. 2. The MF calculates a discrete-time correlation between the received signal and the *PN* code sequence according to the following equation:

$$\text{Correlation} = \sum_{i=1}^{n} S(i)\,PN(i)$$

where $S(i)$ is the chip-rate sampled values of the received signal, $PN(i)$ the *PN* codes taking the binary value of +1 or −1, and n the chip length of the *PN* code sequence.

The received analog voltage is sequentially stored in an analog memory attached to each matching cell. When all the memories are filled with the received signals, they are overwritten with the new data from the oldest. Therefore, the stored analog data are not shifted for the matching. Instead, the *PN* code sequence is shifted against the stored received signals in order to calculate the

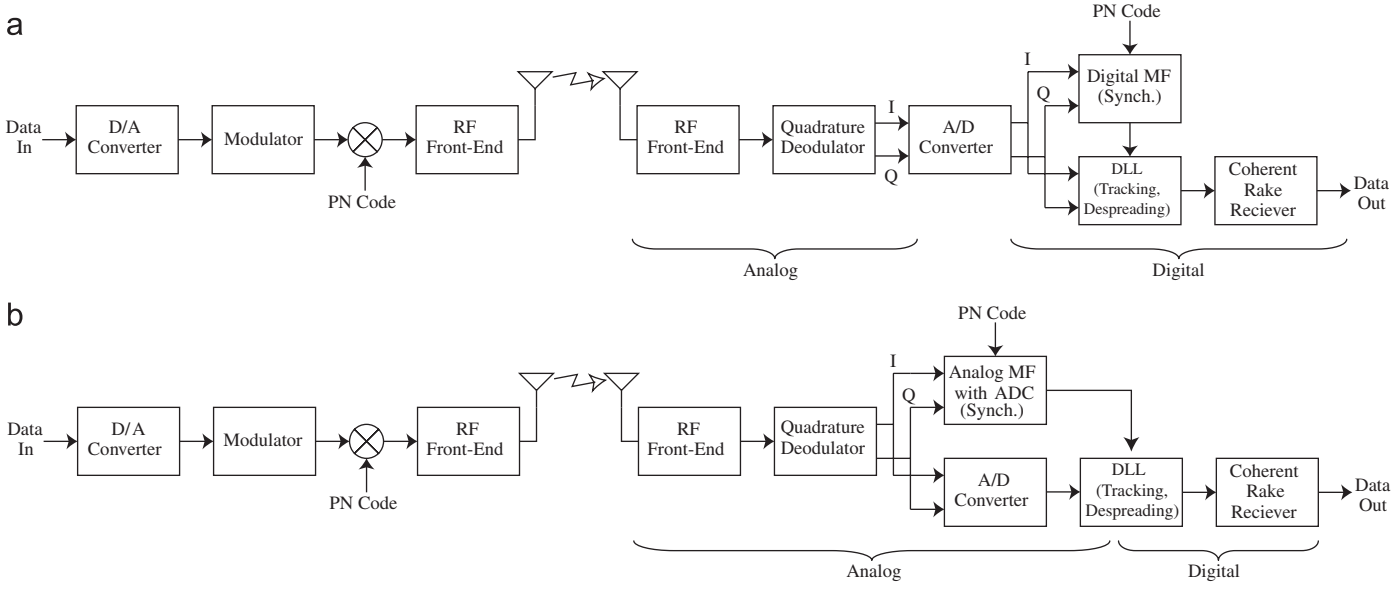

Fig. 1. Simplified block diagram of CDMA systems: (a) conventional and (b) our proposal. In our MF, correlation between the received signal and the *PN* code is calculated in analog the domain. Then, correlation values are converted to digital signal with moderate accuracy.