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Full reliability study of advanced metallization options for 30 nm ½pitch interconnects

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ABSTRACT

Different metallization options that allow filling 30 nm ½pitch interconnect trenches have been explored and their full reliability performance has been benchmarked to conventional PVD TaNTa/PVD Cu seed based metallizations. CVD Co as seed enhancement layer shows no deterioration in barrier performance and improved electromigration performance, but the activation energy for electromigration was 0.68 ± 0.20 eV, which is at the lower end of the expected value of 0.85–0.95 eV for this parameter. When integrating our trenches in a k = 3.2 non-porous SiCOH low-k material, PVD RuTa barriers with 90%Ru and 10%Ta show degraded barrier performance and significant lowering of activation energy for electromigration (0.59 ± 0.05 eV) while when using SiO_2 as intermetal dielectric, no significant reliability deterioration is observed. Finally, it is shown that, using an optimized PVD Cu seed, standard PVD TaNTa-barriers give excellent barrier performance and that typical electromigration lifetime specs can be met with this metallization scheme down to 30 nm ½pitch.

1. Introduction

Shrinking transistor dimensions require scaled BEOL interconnects, where future technologies call for critical dimensions below 30 nm [1]. As operating voltages do not decrease proportionally with these critical dimensions, current carrying capabilities can only be guaranteed by increasing the aspect ratio (AR) of the interconnect. Void-free filling with PVD TaNTa metallic barrier, PVD Cu seed and ECP has been achieved for line dimensions compatible with earlier technologies with line dimensions above 45 nm.

In order to produce void-free Cu wires and via's, a continuous copper seed is required. Due to line-of-sight deposition of the PVD Cu seed, pinch-off is a concern in small dimensions. This is addressed by reducing the Cu seed thickness to a degree that the continuity of the seed at the sidewall of the damascene structures may be compromised. In order to ensure plating at sites where the Cu seed may be defective, a platable repair layer is inserted before copper seed.

PVD RuTa has been proposed as alternative barrier [2,3] and CVD Co was recently put forward as seed enhancement layer [4,5] where improved trench filling was demonstrated. However, only limited reliability experiments were presented and comprehensive time dependent dielectric breakdown (TDDB) and electromigration (EM) results were not shown.

In this paper, we summarize a detailed study where standard PVD TaNTa + PVD Cu seed is compared to the following advanced metallization options: (a) PVD RuTa + PVD Cu seed and (b) PVD TaNTa + CVD Co + PVD Cu seed. For each of these metallization options, a full reliability screening including TDDB and EM failure times and acceleration factors will be presented.

2. Experimental

30 nm ½pitch single damascene lines were integrated using a double patterning scheme [6]. Test structures to study TDDB were on-pitch 1 mm long parallel lines, while for EM, off-pitch 800 μm long single damascene lines with a width of 35 nm were used as test structure.

Table 1 shows the different splits considered in this study. The first two metallization schemes have standard metallization with a 1.5 nm PVD TaNTa and standard Dep. Etch Cu seed. The difference between the splits is in the AR. Next, a 1.5 nm RuTa barrier with 90% Ru and 10% Ta is considered. Such high concentrations of Ru are needed to ensure plating capabilities. In the next metallization scheme studied, a 2 nm CVD Co seed enhancement layer is added to the standard 1.5 nm TaNTa barrier. Finally, an optimized Cu seed is explored where a Cu flash is added to the standard Dep. Etch seed process to repair a possibly defective seed. All above

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Table 1
Studied splits using the 30 nm ½pitch single damascene test vehicle.

Split	Barrier	Seed	AR
TaNTa_Low AR	PVD TaNTa	Dep. Etch	2.5
TaNTa_High AR	PVD TaNTa	Dep. Etch	4
RuTa	PVD RuTa	Dep. Etch	4
TaNTa + CVD Co	PVD TaNTa + CVD Co	Dep. Etch	4
Opt. TaNTa	PVD TaNTa	Dep. Etch + Flash	4

Table 2
Studied splits using the 90 nm ½pitch dual damascene test vehicle.

Split	Barrier	Seed
TaNTa	PVD TaNTa	Dep. Etch
RuTa_Thin	4 nm PVD RuTa	Dep. Etch
RuTa_Thick	8 nm PVD RuTa	Dep. Etch
TaNTa + RuTa	PVD TaNTa + 8 nm PVD RuTa	Dep. Etch

mentioned schemes were integrated in a $k = 3.2$ non-porous SiCOH low-k material as intermetal dielectric (IMD). Also, the "TaNTa_-High AR" and "RuTa" scheme have been integrated in SiO_2.

To build up a deeper knowledge of the behavior of the RuTa-barrier, dual damascene lines with line widths of 100 nm have been integrated. EM structures were single 90 nm via, 900 µm long lines with splits on M2 (Table 2), where upstream EM was performed to study voiding in the layer with the experimental splits.

The first metallization scheme in Table 2 is the reference. The next two schemes are with PVD RuTa barriers with different thicknesses, while the last metallization scheme considers a known good barrier (PVD TaNTa) deposited underneath the experimental RuTa barrier. This split allows investigating the intrinsic RuTa/Cu-interface. All above mentioned metallization schemes were integrated in a porous ($k = 2.5$) SiCOH low-k material. Also, the "RuTa_thick"-metallization was integrated in SiO_2. To facilitate integration, this split was introduced at the M1-level and thus the electromigration performance was studied in the downstream mode.

TDDB-tests were done at wafer level at 100 °C. The voltage dependence of the median failure times, $t_{50\%}$, was fitted using the power law:

$$t_{50\%} \sim V^n, \tag{1}$$

where n is the acceleration factor. Although the power law is not the preferred lifetime model for BEOL TDDB, it offers the advantage that its acceleration factor n does not depend on the spacing between different metal lines. As the different metallization schemes in Table 1 were explored during difference phases of the patterning development, this spacing is not exactly known for our devices. Hence, only the power law allows a fair comparison of acceleration factors and thus it is the preferred model for our analysis.

EM-tests were done at package level at temperatures ranging from 175–330 °C. Temperature dependence of the MTF, $t_{50\%}$, is modeled using the Arrhenius model:

$$t_{50\%} \sim \exp\left(\frac{E_a}{k_B T}\right), \tag{2}$$

where k_B is Boltzmann constant and E_a the activation energy for EM.

3. Results and discussion

Fig. 1 shows a probability plot of the normalized sheet resistance Rs of the 30 nm ½pitch lines for the splits with AR = 4 considered in Table 1. The experimental metallization schemes equally

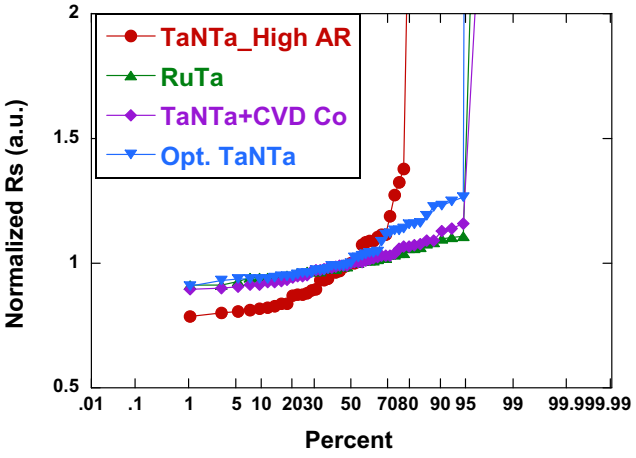

Fig. 1. Normalized Rs for the different splits with AR = 4 from Table 1.

outperform the standard metallization. This confirms existing literature on RuTa and TaNTa + CVD Co down to 30 nm ½pitch where improved yield is reported with these two metallization options [2–5]. Also, adding a Cu flash to the standard Dep. Etch demonstrates its effectiveness to repair defective Cu seeds.

Fig. 2a shows the median failure times after TDDB versus applied voltage V for the standard PVD TaNTa barrier, the RuTa barrier and the PVD TaNTa + CVD Co seed enhancement layer when using the $k = 3.2$ IMD. By adding the CVD Co field enhancement

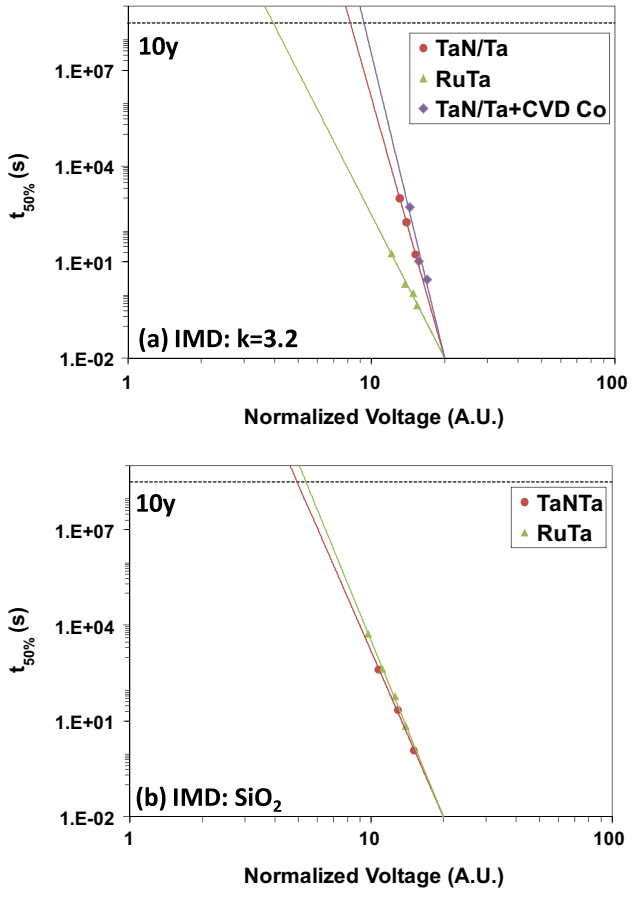

Fig. 2. $t_{50\%}$ versus applied voltage. IMD used was (a) a $k = 3.2$ non-porous low-k material and (b) SiO_2.