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Statistical power supply dynamic noise prediction in hierarchical power grid and package networks

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Abstract

One of the most crucial high performance systems-on-chip design challenge is to front their power supply noise sufferance due to high frequencies, huge number of functional blocks and technology scaling down. Marking a difference from traditional post physical-design static voltage drop analysis, *a priori dynamic voltage drop* evaluation is the focus of this work. It takes into account transient currents and on-chip and package *RLC* parasitics while exploring the power grid design solution space: Design countermeasures can be thus early defined and long post physical-design verification cycles can be shortened. As shown by an extensive set of results, a carefully extracted and modular grid library assures realistic evaluation of parasitics impact on noise and facilitates the power network construction; furthermore statistical analysis guarantees a correct current envelope evaluation and Spice simulations endorse reliable results.

Keywords: Interconnects; Power supply noise; IR drop; Switching activity

1. Introduction

The urgency to integrate increasing amount of functional units in the same circuit enhances the system-on-chip (SoC) scenario design complexity. One of the most critical concern is related to the routing and sizing of interconnects delivering both signal and power supply to the functional units. In fact the compelling scaling down of transistors feature sizes that allows to achieve the SoC integration level is strictly entangled with signal and power supply integrity issues which are aggressively challenging the design of interconnects systems. In particular the *Vdd* and *Gnd* signals are exposed to deviation from the nominal values because of the mutual impact of two factors: the increasing currents to be delivered to the huge number of active devices and the parasitics of both on-chip and package-to-die wires, which are less negligible due to scaling down and to rising frequencies.

The phenomena at the basis of power supply noise (PSN) are voltage drop (*IR* drop) and switching noise ($L\,\mathrm{d}I/\mathrm{d}t$) [1]. The former is due to the high amount of current needed by the power hungry blocks and to the wire resistance. This has the tendency not to decrease proportionally in scaled technologies. The tradeoff between interconnect density requirements, urging toward smaller wires, and the material and geometrical countermeasures, proposed by process engineers, is the key for limiting the *IR* drop impact in future technology nodes. The latter is related to the increasing current transients allowed by scaled transistors and required by frequency constraints in performance compelling applications. In addition, the inductive behavior of interconnects is less and less negligible as frequencies increase, thus enhancing the jeopardizing effect of switching noise.

Both *IR* drop and $L\,\mathrm{d}I/\mathrm{d}t$ are related to on-chip power supply network as well as to package-to-die power delivery system. As reviewed in [2], the package level parasitic inductance has traditionally dominated the power distribution network total inductance. On the contrary, the on-chip wire resistance has been in the past years recognized as having the most aggressive impact on the total PSN drop amount. This classification seems no more suitable to modern high-performance SoCs, as the forecasted increase

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rate of transient current is more than double the average current one [3]. Furthermore, the use of flip-chip package technology in substitution of wirebonding (WB) balances the on-chip/package inductance impact ratio. These aspects imply that switching noise will be in the future less negligible with respect to *IR* drop [4], and that on-chip and package parasitics have influences on PSN which are difficult to disentangle [5–7].

An evolved PSN classification has been recently introduced: It differentiates the static voltage drop (SVD), that is $I_{avg}R$, associated to the *average* gate/block current, from the dynamic voltage drop (DVD), that is $i(t)R + L(\mathrm{d}i(t)/\mathrm{d}t)$, due to *transient* gate/block current. The latter includes not only resistive drop, but switching noise and thus on-chip and package inductive impact as well. DVD evaluation is considered at the time of writing the most trustworthy indication of PSN, as it accurately takes into account transient currents. In fact, it has been shown in [8] that the use of an average *IR* drop for all the gates in a circuit using corner analyses (worst/best case power supply voltage) or the derating factor methodology (gate delay linearly varying with average power supply voltage variation) leads to completely inaccurate results in terms of circuit timing analysis. For example, in a medium performance industrial design (340K gates), synthesized using a 0.13 μm technology, the critical path analysis performed using the derating factor method leaded to approximately 50% underestimation of the noise effect on timing, if compared to an accurate transient Spice simulation. It is thus indubitable the importance of taking into account transient currents for both *IR* drop and switching noise when evaluating PSN effects.

Another important point concerns the design flow stage in which PSN is taken into account. Traditional design methodologies use as much as possible predefined and overdesigned power grids. This is risky in current and future technology nodes, and not practicable in crowded high performance modern designs, in which interconnect resources must be carefully assigned. In more accurate design methodologies physical designers create the power network, verify with back-end tools the power supply voltage variations and adjust the power grid sizes and/or the blocks placement. In high performance design this is not a one shot phase; on the contrary it is cycled many times till the constraints are met, leading to intolerable time-to-market delays. Even if this back-end accurate analysis phase cannot be avoided, a prediction of the power grid design criteria would aid the designer in closing the loop in a shorter time. This is still more important when not only the on-chip power network impact on supply noise is considered, but when the WB or flip-chip influence is taken into account as well. As a matter of fact, the choice on the connection points between package and on-chip grid, their parasitics and layout impact mutually on PSN. In fact, even if an on-chip power grid has been accurately designed, its DVD performance may be completely harassed in case package parasitics are included in the analysis. At the time of writing the possibility to know the DVD amount and its connection with power grid parameters is bounded to the back-end analysis. This means that a post physical-design netlist must be extracted (for both interconnects and logic gates) and a time consuming vector based spice-like simulation must be executed. If, on the one hand, this step is sometimes feasible as a final verification step, on the other hand it is not suitable to a trial-and-error design method. Furthermore, the package impact is often neglected at this design stage. The aim of this work, thus, is to asses noise statistics and their dependency on package and on-chip design parameters. Furthermore, a methodology for estimating in an early design phase the potential DVD and its relation to the design variables is proposed. The solution space can be thus explored before the physical-design step is taken. In this way, when designing the on-chip power grid, near-to-optimal solution criteria can be adopted, and rapid design closure can be achieved. The prediction regards dynamic voltage drop and concerns technology node, geometry, topology and on-chip and package power supply design alternatives.

The rest of the paper is organized as follows: In Section 2 previous works on the subject are reviewed and in Section 3 the proposed methodology is described. In Section 4 the structure used for the PSN evaluation is analyzed and in Section 5 the achieved results are discussed. Conclusions are drawn in Section 6.

2. Previous works

The most important PSN aspects to be analyzed are: power supply network electrical behavior, current envelopes flowing through metal lines, power grid topology and its connection to package, package type and parasitics.

In most of the works addressing PSN analysis, power supply grid parasitics are initially extracted and subsequently the correspondent network is, in most of the cases, simplified to reduce the computational resources necessary for executing the electrical simulation. The challenging tasks do precisely concern both parasitics extraction accuracy and power grid modeling. The goal is to achieve a good trade off between precision, and thus results reliability, and the possibility to reasonably manage the extracted grid complexity. This step has been in past works reached focusing on different methodologies. They concern the way in which the grid parasitics can be extracted and the fact that parasitic extraction can be pursued considering or neglecting the inductance (*RLC* vs. *RC* parasitic networks). For example, in [9] macro-models for grid subsets are created, while in [10] the grid is reduced to a coarser structure mapped back to the original grid. In [11,12] the grid is modeled using transmission line theory and, in particular, in [4] lossy transmission lines are used for modeling power grid blocks with frequency dependent properties. In [13] a finite difference time domain method is