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Surface potential mapping of p^+/n-well junction by secondary electron potential contrast with *in situ* nano-probe biasing

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ABSTRACT

This article investigates the surface potential distribution of a biased p^+/n-well diode using secondary electron potential contrast (SEPC) with an *in situ* nano-probe trigger. The SEPC image is digitized and quantified for the conversion of the image contrast to the voltage scale, allowing for the identification of the depletion region and the electrical junction. The overlap length between the poly silicon gate and the p^+ region is also depicted by two-dimensional (2-D) imaging. This study demonstrates that the proposed *in situ* nano-probe system is highly effective for surface potential mapping.

1. Introduction

Semiconductor device performance is determined by the distribution and concentration of the dopant [1,2]. The 2-D junction profile technique has become vital to the development of nano-scale devices. Many studies have investigated the junction profile through various methods including secondary ion mass spectrometry (SIMS) [3], chemical delineation [4,5], scanning capacitance microscope (SCM) [6], Kelvin force probe microscope (KFPM) [7], and electron holography [8,9]. KFPM and electron holography depict the junction profile through surface potential mapping [7–9]. KFPM uses a tiny probe to scan across the junction and measure the long range electrostatic potential interaction between the probe and specimen surface. Off-axis electron holography reconstructs the electrostatic potential distribution across a diode based on electron interference.

Recent research has proposed the use of secondary electron potential contrast (SEPC) to inspect junction profiles with a sensitivity ranging from 10^{16} to 10^{20} cm^{-3} and a spatial resolution of 10 nm [10–14]. Since 1960, researchers have been investigating the mechanism of dopant contrast in scanning electron microscope (SEM). Various studies have investigated factors that influence dopant contrast. Perovic et al. and Turan et al. proposed that surface potential determines the secondary electron emission rate [15,16]. Sealy et al. proposed that the presence of a three-dimensional field outside the specimen is a major factor in dopant contrast [17]. Hsiao et al. studied strain effects in dopant contrast enhancement [18]. Elliott et al. and Venables et al. reported that the SEPC profile of a p^+/n-well junction shows a linear relationship with the logarithm of the SIMS depth profile [10,11]. Elliott's study on a biased junction found that the SEPC intensity is proportional to the built-in voltage [10].

Though the above-mentioned studies show that SEPC is a promising technique for junction profiling, few applications for SEPC in the junction profiling of actual circuits have been reported, probably because SEPC is difficult to observe in site-specific locations due to the reduced SEPC signals under standard SEM conditions. Sealy et al. suggested that surface band bending on a cleaved diode will reduce the dopant contrast [17]. Recent site-specific studies suggest that FIB sample preparation may indeed facilitate the inspection of dopant contrast [19]. During sample preparation, however, damage to the surface layer has been reported to reduce dopant contrast [19] and, in the worst case, SEPC cannot be observed by SEM imaging [20]. Hence, this study fills a gap in the literature by investigating solutions for enhancing dopant contrast by the *in situ* bias of the diode with nano-probe tips. The specific aims of this report are (a) to enhance dopant contrast with nano-probe assistance, (b) to link the image contrast to a voltage scale, and (c) to elucidate theoretical assumptions about the device physics. The proposed solution may also serve as a basis for further studies of SEPC mechanisms with static triggers. The simplicity of the method should enable its widespread adoption in dopant profile inspection.

2. Experimental

The experimental specimen was a functional static random access memory (SRAM) module manufactured with 90 nm IC tech-

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nology, on a p-type (100) silicon wafer substrate with 8–12 Ω cm resistivity. After patterning the active area, implantation procedures formed the well and plus regions. Thermal activation at 1000 °C for 5 s and metallization were carried out sequentially as formal procedures. An SRAM chip with normal functionality was fabricated and manually polished with an Allied Multiprep™ to enable cross-sectional observation by SEM. In this work, the specimen is an SRAM chip with one poly layer and five metal layers. The diamond film was changed from coarse to fine to minimize scratching of the specimen surface. The specimen was prepared in cross-section for dopant profile inspection.

All SEM images in this paper were obtained with a Hitachi S4800 equipped with an $E \times B$ filter. The typical secondary electron (SE) energy is smaller than 50 eV. The $E \times B$ filter removes the high energy tail of the backscattered electron (BSE) and guides SE to the upper detector to enhance the SEPC effect on the silicon. The SEM operating conditions were optimized to visualize the diode. The image was acquired with a 1 keV primary electron energy at a working distance of 6 mm.

Despite the $E \times B$ detector's enhancement of the SEPC image, surface band bending and damage to the surface layer could reduce SEPC and limit its application in real circuits. To minimize the contrast reduction effect from these factors, a nano-probe system was installed in the SEM chamber. The junction condition was reverse-biased with a four-micromanipulator nano-probe system mounted to the Hitachi S4800 stage. The nano-probe tip had a 50 nm radius and could probe any node found in the SEM image. Fig. 1 depicts a partial cross section of the SRAM chip to schematically illustrate the SEPC inspection procedure, and three p^+/n-well junctions, two polycrystalline Si gates, and a nano-probe tip probe are shown in the middle of a p^+/n-well node. The middle p^+/n-well node serves as a positive node (V_{dd}) for SRAM and connects to the n-well through metal routing. The other two p^+/n-well nodes serve as the SRAM drain node. The middle p^+/n-well junction was electrically biased with a trigger voltage of 1 V. The p-substrate was kept in the ground state. The colors of the left and right p^+/n-well junctions and p-substrate illustrate the dopant contrast after bias voltage was applied.

3. Results and discussion

Fig. 2 shows an SEM image corresponding to the setup illustrated in Fig. 1. The nano-probe tip was applied to the middle p^+/n-well node with positive 1 V and the p-substrate with the ground. Because the middle p^+/n-well node, serving as an SRAM V_{dd} node, was connected with the n-well through a metal layer, thus the surface potential of the n-well will also be positive 1 V. The figure shows high contrast in the p-substrate and p^+ region, and low contrast in the n-well region. Fig. 3 presents a magnification of the SEPC image shown in Fig. 2. Two poly silicon gates and three p^+/n-well junctions are visible. The left and right p^+ regions show high contrast. The figure not only clearly shows the p^+ regions, but also the lightly-doped drain region (p^- region), thus confirming the good spatial resolution of the SPEC method. Contrast is low in the middle p^+ region since it acts as an SRAM V_{dd} node and is connected with the n-well region with positive 1 V. Additionally, the absence of doping contrast was restored when the bias voltage was triggered in the junction, indicating that SEPC is affected by the surface potential of the specimen.

The nano-probe system can assist the application of the p^+/n-well junction nodes in a reverse biased condition. Fig. 4 shows the intensity profile of the p^+/n-well diode with trigger voltages of 0 V on the p^+ node and 1 V on the n-well nodes. To further elucidate the device physics, a series of data analyses of p^+/n-well intensity profiles were performed. Each point in the intensity curve is the average of four of its adjacent points. The intensity curve was

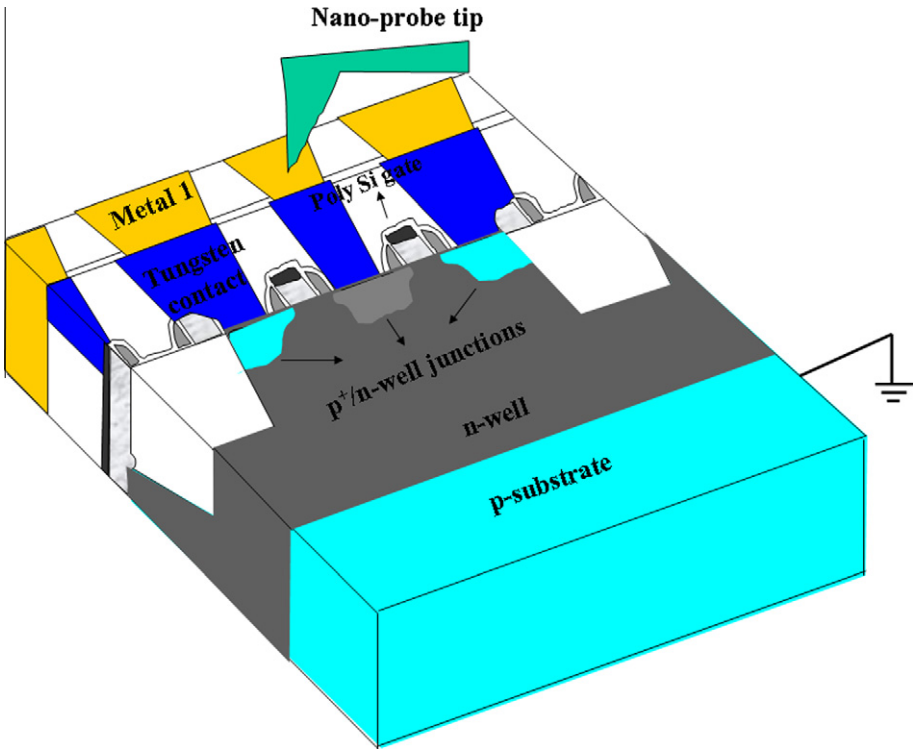

Fig. 1. A partial cross-section of the SRAM chip schematically illustrates the SEPC inspection; three p^+/n-well junctions, two polycrystalline Si gates, and a nano-probe tip are shown. The middle p^+/n-well junction was electrically biased with a trigger voltage 1 V. The p-substrate was kept on the ground state. The colors of the left and right p^+/n-well junctions and p-substrate illustrate the dopant contrast after electricity was biased. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)