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Ground plane fin-shaped field effect transistor (GP-FinFET): A FinFET for low leakage power circuits

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ABSTRACT

In this paper, a fin-shaped field effect transistor (FinFET) structure which uses ground plane concept is proposed and theoretically investigated. The ground plane reduces the coupling of electric field between the source and drain reducing drain-induced barrier lowering (DIBL). To assess the performance of the proposed structure, some device characteristics of the structure have been compared with those of silicon on insulator-FinFET (SOI-FinFET) and Bulk-FinFET structures (where the BOX layer covers all the regions except the channel region). In addition, we compare different characteristics of static random access memory (SRAM) cells based on the proposed device structure as well as SOI-FinFET and Bulk-FinFET structures. The characteristics include standby power consumption, and read static noise margin (SNM). Finally, the behavior of the proposed device in the presence of dimensional variations (channel length and thin film thickness variations) and random dopant fluctuation (RDF) are studied and compared with those of the other two structures.

1. Introduction

For nano-scale metal oxide semiconductor field effect transistor (MOSFET) devices, the undesired effects of short-channel-effects (SCEs) induced by decreased gate control become critically important. To minimize these effects, several double and multi gate structures have been proposed. Among them, fin-shaped field effect transistors (FinFETs) have higher immunity to SCEs, quasi-ideal subthreshold-swing (SS), high mobility of carriers and high saturation-current [1]. FinFETs have proposed with different device structures including double-gate [2], Pi-gate [3], surrounding-gate [4], gate all-around [5], and omega-gate [6]. The structures can be fabricated on both silicon on insulator (SOI) and bulk-wafers. SOI-FinFETs have shown several advantages over Bulk-FinFETs such as less leakage current, less source-body and drain-body capacitances (C_{SB} and C_{DB} respectively) [7,8], higher saturation current, better subthreshold behaviors [9,10], and less sensitivity to the substrate-doping. On the other hand, Bulk-FinFETs have the advantages of lower cost of fabrication [11,12], lower defect density, low self-heating, and more stability against negative-bias-temperature instability (NBTI) [13].

Among important short-channel-effects, drain-induced barrier lowering (DIBL) significantly affects the ability to turn off the transistor by the gate voltage even in these new gate structures. In long-channel SOI devices, the subthreshold slope can be increased by increasing the buried oxide (BOX) thickness [14]. In short channel transistors, with increasing the BOX layer thickness, the subthreshold slope decreases [15]. This is due to the enhanced DIBL effect induced by more penetration of the electric field into the BOX layers. The ground plane (GP) technique is one of the methods used to reduce the DIBL effect in short-channel SOI structure [16–18]. It is effective only when the distance between the GP and the drain is small compared to the channel length [15]. In [15], two different methods have been used in applying the GP technique to the SOI structure. The methods use the GP in the substrate (GPS) and in the buried-oxide (GPB). The results presented in [15] for the GP structures showed lower leakage power consumption compared to that of the structure without ground planes.

In this paper, we propose a FinFET device structure that invokes two ground planes under the source and drain for reducing the DIBL effect. The purpose of this paper is to study a new structure whose difference with the conventional Bulk-FinFET are the use of a BOX layer and buried GP layers. Also, its difference with the SOI-FinFET structure which has the BOX layer is the buried GP layers. In Section 2, we describe the proposed structure and compare its characteristics with those of SOI-FinFET and Bulk-FinFET structures. In Section 3, we study the effects of channel doping density and channel length on device characteristics of the proposed structure. In Section 4, the performance of this structure when used in a real application such as static random access memory (SRAM) cells is investigated. Then, the efficiencies of the structures in the

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presence of process variations are investigated in Section 5. Finally, the conclusion of the paper is given in Section 6.

2. Proposed GP-FinFET structure

In this work, we compare the proposed structure with two conventional FinFET structures (SOI-FinFET and Bulk-FinFET) using 3D simulations. In SOI-FinFET, the channel and substrate are isolated by a BOX layer while in Bulk-FinFET the BOX layer covers all the regions except the channel region (similar to the structures of, e.g., [19,20]). The proposed ground plane FinFET (GP-FinFET) structure is similar to SOI-FinFET structure except for the two ground planes and polysilicon layer inside the BOX layer. The fabrication steps for SOI-MOSFET with two ground planes inside the BOX layer are described in [15] as follows: The structure with ground planes can be realized using the SOIAS technology with the bonded-SIMOX approach. By ion implantation of boron through the silicon film in two masking steps, the formation of p^+ islands and insulation of these islands with polysilicon after thermal anneal, we can form the ground planes. By self-aligned process with the gate-side spacer, the ground plane can be fabricated after the gate-electrode etching. In order to control the electric field around the junction regions, the ground planes are placed under the source and drain regions.

Fig. 1 shows a 3D view of the proposed structure which has the ground planes under source and drain where the vertical distance between source/drain and ground-planes are denoted by X. Unless stated otherwise, the doping densities and the dimensions shown in Fig. 1 may be assumed as those given in Table 1. Also, we assumed a maximum aspect ratio ($H_{Channel}/t_{Si}$) of 5 to obtain the larger saturation drain current [21,22]. Note that in the proposed structure, because of short fin length and use of tri-gate structure, the corner effects may influence the electrostatic potential profile between the gates and source/drain more than those of SOI-MOSFETs studied in [15]. Following the suggestion in [23], in the structure used in this work, we have used tall spacers to reduce the corner effects. Our simulations shows that even without tall spacers, the corner effects are negligible. To achieve about the same on-state performances for Bulk-FinFET and SOI-FinFET, the bulk device should have a lightly doped (or undoped) body [24,25]. For these devices, the threshold voltage control may be performed by the metal gate which has the midgap work function (4.6 eV) [24,25]. Therefore, we used the undoped channel and substrate along with the metal gate which covers three sides of the channel.

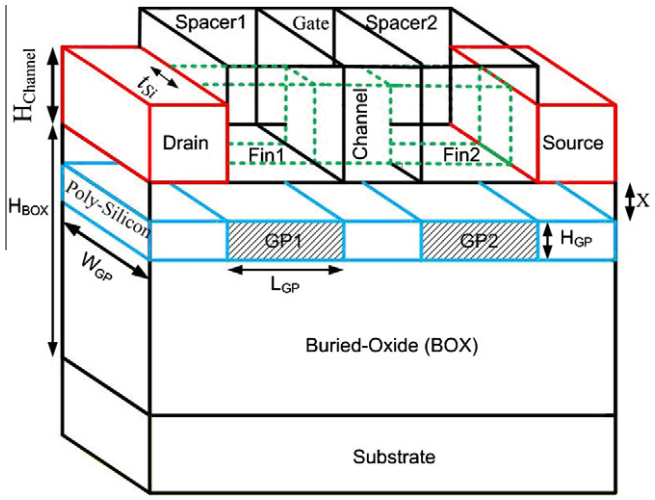

Fig. 1. 3D view of the proposed structure with ground planes.

Table 1
Main parameters of the three structures.

Parameter	Value
Gate oxide thickness	2 nm
X	10 nm
$L_{Channel}$	50 nm
H_{BOX}	100 nm
$H_{Channel}$	100 nm
L_{GP}	125 nm
H_{GP}	20 nm
t_{Si}	20 nm
W_{GP}	500 nm
Source/drain doping	1×10^{20} cm^{-3}
Channel doping	1×10^{15} cm^{-3}
Gate work function	4.6 eV

To select a proper ground plane width (W_{GP}), we simulated the structures with different ground plane widths. The results showed that when the ground plane width equaled to the source/drain width, a better control of the electrostatic potential of the channel (by the gate) was obtained. When the ground plane width was smaller than that of the source/drain, the electrostatic potentials beneath the source/drain were not fully grounded degrading the control of the channel electrostatic potential. The 3D simulations were performed using Sentaurus-Device simulator [26]. The models considered in our simulations included doping dependence model, high field saturation model, and vertical electric field dependence model (Enormal model) for mobility and Shockley–Read–Hall model for recombination. The density gradient transport model, which solves the quantum potential equations self-consistently with the Poisson and carrier continuity equations, was also used for transport [26]. Finally, note that we have compared the intrinsic structures of the devices, and therefore, did not consider any contact resistance model.

The electrostatic potentials of GP-FinFET, SOI-FinFET and Bulk-FinFET are shown in Fig. 2. As the results show, the impacts of the source and drain potentials on the channel electrostatic potential in the GP-FinFET are minimized. This is achieved by grounding the electrostatic potential beneath the source and drain using the ground planes in the proposed structure. Therefore, it is expected that the DIBL is minimized in this structure (see Fig. 5b). The drain current (I_D) versus the drain (V_{DS}) voltage characteristics at a constant gate overdrive voltage ($V_{GS} - V_{th}$) for the structures are shown in Fig. 3. In the case of the constant gate overdrive voltage, the drain current of GP-FinFET is larger than those of the other two devices at the high drain voltages. The results show that the saturation region for the GP-FinFET device occurs at a higher drain voltage. The higher drain saturation voltage may be attributed to a smaller velocity saturation effect for a given drain-to-source voltage in the case of GP-FinFET. This is due to the use of the ground planes which lower the strength of the electric field induced by the drain-to-source voltage. The subthreshold characteristics ($I_D - V_{GS}$) for the structures are shown in Fig. 4. The results indicate a larger subthreshold slope (less subthreshold-swing) for the proposed structure compared to those of the others. This leads to a considerable reduction in the leakage current. Therefore, the ratio of the ON current to OFF current for the proposed structure is larger than those of the other two structures.

In this work, the threshold voltage (V_{th}) is the gate voltage at which the drain current is equal to $10^{-7}W/L$ [A] where W is the effective width of the gate and L is the channel length [27,28]. DIBL and subthreshold-swing are calculated, respectively, using [15,29,30]

$$\mathrm{DIBL} = \frac{V_{th}(V_{DS} = 1\ \mathrm{V}) - V_{th}(V_{DS} = 0.05\ \mathrm{V})}{V_{DS}(= 1\ \mathrm{V}) - V_{DS}(= 0.05\ \mathrm{V})} \quad (1)$$