Microelectronic Engineering 95 (2012) 112–115

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Fabrication and electrical characteristics of the Pt/SiNWs/*n*-Si/Al Schottky diode structure

Meiguang Zhu [a,b], Jian Zhang [b,*], Huina Hou [b]

[a] Shanghai Precision Metrology and Testing Research Institute, 3888 Yuanjiang Road, Shanghai 201109, China
[b] Department of Electronic Engineering, East China Normal University, 500 Dongchuan Road, Shanghai 200241, China

ARTICLE INFO

Article history:
Received 23 December 2010
Received in revised form 5 December 2011
Accepted 13 February 2012
Available online 21 February 2012

Keywords:
Silicon nanowires
Pt/SiNWs
Schottky diode
Optimal conditions

ABSTRACT

Array-ordered silicon nanowires (SiNWs) were fabricated directly on *n*-Si substrate by wet chemical etching. The electroless plating method was used to modify SiNWs with platinum (Pt) nanoparticles as the top electrodes, forming the novel tridimensional Pt/SiNWs/*n*-Si/Al Schottky diode structure. The structural and electrical characteristics were investigated to obtain the optimal experimental conditions for forming the Pt/SiNWs/*n*-Si/Al Schottky barrier diode structures. Three key electrical parameters (ideality factors, barrier heights and series resistance) are 11.58 eV, 0.93 eV and 1.99 kΩ, respectively. The study reveals that the Pt/SiNWs/*n*-Si/Al Schottky diode structure would have a great potential application in nanoscale optoelectronic devices by controlling the experimental parameters properly.

1. Introduction

Metal–semiconductor (MS) Schottky barrier diodes play an important role in the modern semiconductor industry due to their extensive applications in various electronic and optoelectronic devices. The traditional Schottky barrier diodes are based on planar structure. So far lots of investigations on the structure have been carried out [1–4].

Silicon nanowires are considered to the promising building block for the next generation's nanodevices due to their interesting shape-dependent and unique electrical properties [5–8]. Now, the devices based on silicon nanowire employe both the single silicon nanowire and the silicon nanowire arrays [9,10]. For example, the single silicon nanowire has been used as the building block to construct the FET sensors [11]. The silicon nanowire arrays have been employed to develop the sensors [12–14]. However, to the best of our knowledge, works related to the novel tridimensional Schottky barrier diodes based on silicon nanowire arrays are seldom reported.

In the present work, a simple, low cost wet chemical etching method was used to fabricate the large-scaled SiNWs. While, the platinum (Pt) nanoparticles were deposited by the electroless plating process to prepare Pt/SiNWs/*n*-Si/Al structure. The structural characterizations of Pt/SiNWs were examined by scanning electron microscope (SEM), X-ray diffraction (XRD) and transmission electron microscopy (TEM). The electrical characteristics were investigated by current–voltage (*I*–*V*) technique for the Pt/SiNWs/*n*-Si/Al structure formed in different experimental conditions. The diode parameters (ideality factor *n*, barrier height Φ_b, series resistance R_s) were extracted by Cheung's model [15].

2. Experiment

2.1. Silicon nanowires fabrication

Single-side polished *n*-type silicon-wafers (with (100) orientation and ~0.1–10 Ω cm resistivity) were used as the substrates for the preparation of SiNWs. Before etching, the silicon wafers were cleaned carefully via standard RCA process. Then the cleaned silicon wafers were placed into a Teflon etching container which contained a mixture of 35 mM $AgNO_3$ and 15 mM HF. The silicon wafers were etched for 60 min at room temperature under 1 atm. After etching, the samples were taken out and washed with concentrated HNO_3 to remove surface byproduct, Ag nanodendrites. Then the samples were rinsed with DI water and dried with nitrogen carefully. The in-detailed process for SiNWs fabrication can be found in our previous paper [8,16].

2.2. Pt/SiNWs Schottky contact

Prior to the electroless process, the SiNWs samples were treated by dipping into 5% aqueous hydrofluoric acid solution (HF) for 10 s to remove the surface silicon oxide layer. After HF immersion, the SiNWs surface is passivated by hydrogen to form the hydrogen (H)-terminated Si surface, which is particularly resistant to air

* Corresponding author. Tel.: +86 21 54345203; fax: +86 21 54345119.
E-mail address: jzhang0002@gmail.com (J. Zhang).

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doi:10.1016/j.mee.2012.02.009

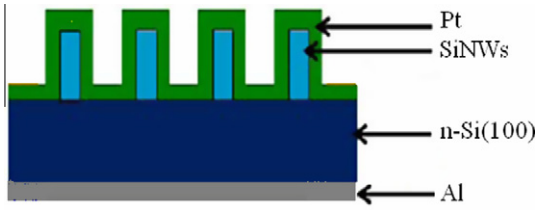

Fig. 1. Schematic of Pt/SiNWs/*n*-Si/Al structures.

oxidation. Then, the samples were immerged into K_2PtCl_6 solutions to form directly the Pt/SiNWs Schottky contact. In the experiment, the K_2PtCl_6 concentration and the deposition time varied, respectively, to investigate their influence on current–voltage characteristics of the Pt/SiNWs/*n*-Si/Al structure.

2.3. Al/n-Si ohmic contact

For current–voltage measurements, an Al layer was thermally evaporated on the backside of the *n*-Si substrate, and then annealed at 450 °C for 3 min in N_2 atmosphere to establish a large area ohmic contact. So the Pt/SiNWs/*n*-Si/Al structures were formed. The schematic of the corresponding SBD structure is shown in Fig. 1.

3. Results and discussion

3.1. Structural characteristics of Pt/SiNWs

Fig. 2 is the SEM image of the Pt/SiNWs nanocomposite structure formed in 10 mM K_2PtCl_6 solutions for 10 min electroless plating time. As can be seen from Fig. 2, the SiNWs are encapsulated by a relatively homogeneous and smooth layer. The result of the X-ray diffraction analysis further illustrates that the outside layer is Pt nanoparticles, just as shown in Fig. 3. Therefore, it implies the Pt/SiNWs structure is fabricated successfully through modifying SiNWs with platinum (Pt) nanoparticles by the electroless plating method.

3.2. The influence of the electroless plating parameters

For electroless plating method, the key parameters are the K_2PtCl_6 concentration and plating time (t). It is found that the two factors can determine the Pt layer thickness and the electrical properties of Pt/SiNWs/*n*-Si/Al structure. So the effect on current–voltage (I–V) characteristics for Pt/SiNWs/*n*-Si/Al structure was investigated. Meanwhile, the corresponding electrical parameters

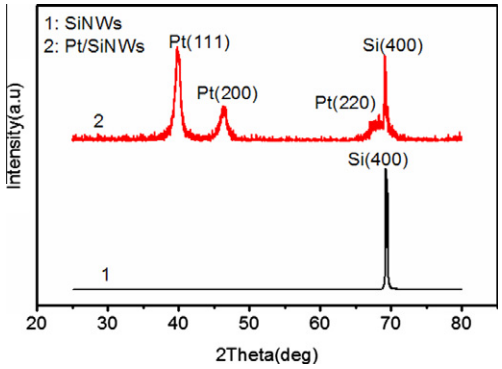

Fig. 3. X-ray diffraction (XRD) image of SiNWs and Pt/SiNWs.

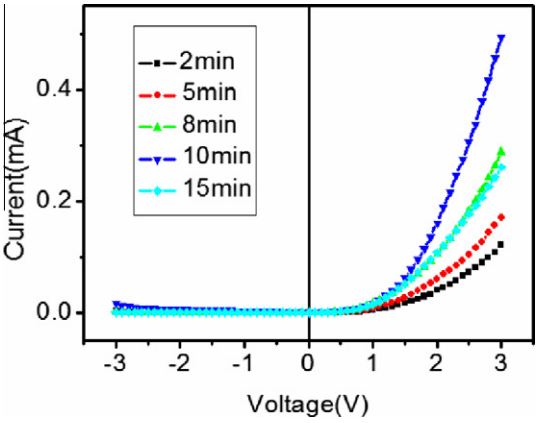

Fig. 4. Current–voltage (I–V) curves measured for Pt/SiNWs/*n*-Si/Al structures which Pt layers formed in 5 mM K_2PtCl_6 solutions for 2, 5, 8, 10 and 15 min, respectively.

Table 1
Experimental I–V characteristics parameters for Pt/SiNWs/*n*-Si/Al structures at different electroless plating time of Platinum (Pt) nanoparticles.

	2 min	5 min	8 min	10 min	15 min
R_s (kΩ)	17.91	15.47	8.24	3.80	6.95

(ideality factor n, barrier height ϕ_b and series resistance R_s) were extracted by Cheung mode to evaluate the influences. Cheung's functions [15] can be written as

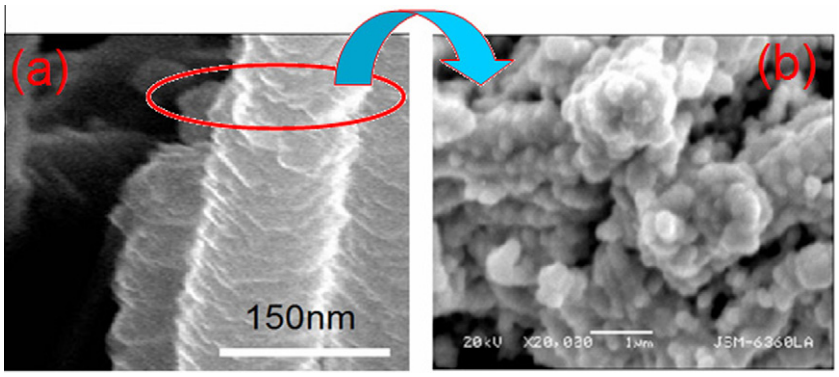

Fig. 2. Scanning electron microscope (SEM) image of (a) Pt/SiNWs nanocomposite structure formed in 10 mM K_2PtCl_6 solutions for 10 min electroless plating time and (b) partial enlarged detail.