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Review Article

Wafer-level three-dimensional integrated circuits (3D IC): Schemes and key technologies

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ABSTRACT

Schemes and key technologies of wafer-level three-dimensional integrated circuits (3D IC) are reviewed and introduced in this paper. Direction of wafer stacking, methods of wafer bonding, fabrication of through-silicon via (TSV), and classification of wafer type are options for 3D IC schemes. Key technologies, such as alignment, Cu bonding, and TSV fabrication, are described as well. Better performance, lower cost, and more functionality of future electronic products become feasible with 3D IC concept application.

1. Introduction

In recent decades, with the development of microelectronic technologies, high performance, small form factor and low cost of electronic products have become basic requirements for surviving in the market. Traditional integrated circuits are fabricated on one flat silicon wafer which the development is restricted by two-dimensional version. In order to follow Moore's law [1], chip makers are trying to integrate many transistors into the chip with better performance. However, when the gate length and oxide thickness of transistors both approach to the physical limit, the two-dimensional scaling will eventually face the end of the road.

Even though the dimensional scaling improves device performance in terms of gate switching speed, it has a reverse effect on global interconnect latency [2]. In addition, the global interconnect may dominate the operation frequency in some cases. Three-dimensional integration is one of the candidates to keep up with Moore's law and solve the issues above. The basic concept of three-dimensional integration is to integrate doubled or more transistors into the same "area". Besides, three-dimensional integration scheme can integrate different ICs from their own optimum processes together without using compromised fabrications which lower the efficiency and the yield [3–5].

From the packaging point of view, multi-chips package is the trend of semiconductor industries. Three-dimensional packaging offers a smaller area solution with lower power consumption. Although three-dimensional integration has many advantages, challenges such as reliability, heat dissipation, and testing methodology are current topics to be solved. This paper reviews and summaries wafer-level three-dimensional integrated circuits (3D IC). The content will focus on different 3D IC schemes and introduce key technologies. The information provides guidelines and references for researchers who are interested in this field.

2. Classification of wafer level 3D integration technology

The concept of 3D IC is based on the new position of ICs: *Z* direction. This means the position of ICs does not limit on *X*–*Y* plan anymore. Therefore we can stack the ICs to shorten the interconnection and also reduce the visible surface which increases the application range due to the small chip size and better efficiency.

3D integration includes three options: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-level 3D integration is different from 3D package technology in terms of the stacking size. Generally speaking, 3D package technology focuses on final IC chip/die stacking. On the other hand, key technologies and schemes of wafer-level 3D integration are completed in wafer level, including bonding technology and through silicon via (TSV).

Because the fundamental concepts of wafer-level 3D integration technologies are the same as those of 3D packaging, this paper will only focus on wafer-level 3D integration. In general, wafer-level 3D integration can be classified into different categories based on the technologies applied.

2.1. Direction of wafer stacking

Based on the stacking direction of two device wafers, there are two different kinds of wafer stacking: face-to-face and face-to-

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back. The effects of wafer stacking direction are very enormous, including the circuit symmetry, fabrication difficulties, capacitance of interconnection and alignment consideration. Both of the stacking methods have been applied in 3D integration applications. Even mutual usage of each stacking method is also possible [6].

2.1.1. Face-to-face

For face-to-face version wafers, two wafers align and bond face to face together with the circuits, as shown in Fig. 1. From the fabrication technology point of view, this kind of integration is easy to be applied and does not need an additional handle wafer. However, the wafer to wafer symmetric issue needs to be taken into consideration. This means while designing the top wafers, since circuits on these wafers will be faced down during bonding, the action of mirroring circuits is required. At the same time, the symmetry and placement of alignment marks of both wafers should be considered as well.

2.1.2. Face-to-back

For face-to-back version wafers, the wafer upward (upper wafer or top wafer) should be thinned from the substrate with the top side attaching to an additional handle wafer. Comparing to the face-to-face version, this approach increases the complexity of process. However, the wafer to wafer symmetric issues can be eliminated. While the handle wafer is transparent and thinned wafer is thinned enough, the alignment process becomes transparent and much easier, as shown in Fig. 2.

2.2. Methods of wafer bonding

Bonding (stacking) technology is the key technology in 3D integration, both in wafer-level and chip-level. This process can make two or more layers stacking in *Z*-direction. Based on the bonding medium, the wafer bonding can be categorized into three options.

2.2.1. Metal-to-metal

Metal-to-metal bonding technique provides good adhesion and thermal conducting due to the characteristics of metal compounds. The use of metal diffusion bonding (thermo-compression bonding) in 3D applications allows the mechanical and electrical connections to be made between two wafers in one step process. For example, copper, tin and gold are usually the materials of metal bonding. The bonding parameters include 150–400 °C bonding temperature, high bond pressure up to 40 kN, high vacuum or nitrogen ambient [7–12]. Copper is one of the popular choices for 3D IC bonding since it is the interconnecting material of the standard CMOS process [7–10]. However, the bonding temperature for metal-to-metal bonding process needs to follow the thermal budget of existing devices and circuits.

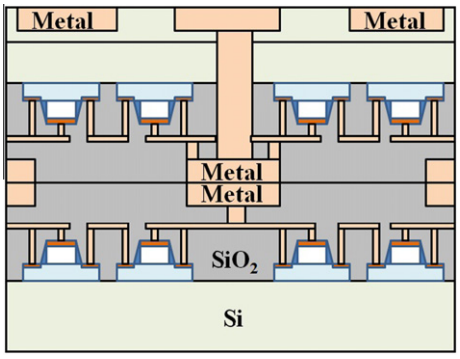

Fig. 1. Face-to-face wafer stacking.

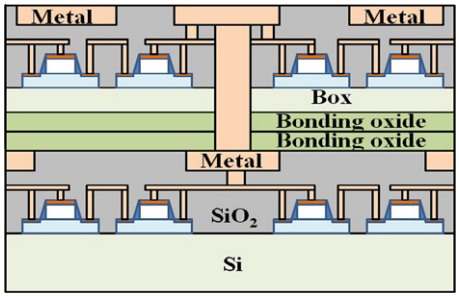

Fig. 2. Face-to-back wafer stacking.

2.2.2. Oxide-to-oxide

Since silicon oxide is the standard dielectric material of semiconductor processing, this material naturally becomes the candidate of bonding medium among two wafers [13–17]. The advantage of silicon oxide adhesion is CMOS process compatible and also gets high stacking density when top wafer is an SOI wafer. However, the oxide surfaces of both wafers should be extremely cleaned and flattened; usually an extra process is required. In bonding process, two-step technique is performed with room temperature contact followed by a high temperature anneal, up to 1000 °C, to let the bonding interface form strong covalent bonds (Si–O–Si) [17].

2.2.3. Polymer-to-polymer

Polymer-to-polymer bonding technique is similar to oxide-to-oxide bonding technique; both of the techniques can have high stacking density with the use of an SOI wafer. Furthermore, polymer-to-polymer bonding technique has better adhesive strength because the polymer material is more compliant than silicon oxide. [18–24]. This advantage is significant for wafer-level bonding. Nowadays SU-8 and BCB (benzocyclobu-tene) are the most common material used for wafer level adhesive bonding in 3D integration and applications [24]. However, the fusion point or glass transition temperature (Tg) of polymer is usually lower than 400 °C, which restricts the following process and even may pollute wafers or instruments due to the decomposition of polymer.

2.3. Fabrication of through-Si-via (TSV)

The order of TSV fabrication is much correlation with the wafer stacking, TSV filling materials, and device fabrications. Generally, the definition of TSV fabrication is based on the order with metal connection fabrication (so called BEOL process). The fabrications of TSV before and after BEOL fabrication are defined via-first and via-last, respectively.

2.3.1. Via-first

Via-first process means the TSVs are fabricated before BEOL process [25–27]. In this scheme, the materials to be filled in TSVs cannot be metals, such as Cu. In addition, because metal levels are not fabricated in this stage yet, the aspect ratio of via-first TSVs is smaller than those of via-last ones. Fig. 3 shows the process of via-first.

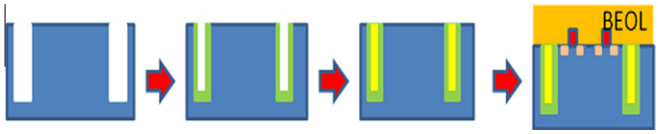

Fig. 3. Via-first process flow.