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Compensation of self-heating-induced timing errors in bipolar comparators

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ABSTRACT

Self-heating effects in bipolar comparators manifest themselves as signal-dependent output signal timing variation. In applications where comparator circuits are used for precise timing measurement of input signal threshold crossings, such as test and measurement instruments, self-heating presents a design challenge that must be addressed. A comparator circuit, utilizing a novel circuit-based self-heating compensation method, has been designed and fabricated in a BiCMOS HBT process. This self-heating compensation scheme differs from previously reported compensation circuitry in that it is designed for the compensation of asynchronous comparators. Measurements presented here demonstrate the effectiveness of the compensation circuitry at reducing self-heating-induced timing errors over a wide range of input signal amplitude and common-mode voltage.

1. Introduction

Comparator circuits used in applications where precise measurement of the timing of input signal threshold crossing is sought (e.g., test and measurement applications, such as oscilloscope trigger comparators) are highly susceptible to the effects of self-heating. This is particularly true of comparator circuits fabricated in bipolar and BiCMOS processes utilizing deep-trench isolation, where large thermal resistances between transistors result in a high degree of differential self-heating – even between closely-spaced devices. Offsets between nominally-matched transistors in a comparator circuit, induced by differential self-heating, yield signal-dependent propagation delay variation through the comparator, and resultant timing errors at the comparator output [1].

Much has been reported in the literature about the modeling of transistor self-heating, [2–7], and many works have examined the effects of self-heating on integrated-circuit building blocks such as current mirrors, e.g. [8–11]. Techniques used in practice for the compensation of self-heating in linear amplifiers, e.g. [12–14], are seldom reported in the literature, and past work done to address the issue of self-heating in comparator circuits has been limited to clocked comparators, used in sampling comparator systems [15–17]. In this work, a self-heating compensation scheme is presented that is applicable to comparator circuits used in asynchronous applications. This compensation scheme utilizes a circuit-based approach, requiring no modification of the standard device cells available within a given process, and is therefore easily ported between IC processes.

The following section of this paper will first provide a general overview of how self-heating affects differential pair amplifiers, a common comparator-circuit building block, followed by a discussion of techniques that can be used to compensate for the effects of self-heating in differential pairs, and finally concluding with a look at self-heating effects and compensation in comparator circuits in particular. A comparator chip, including circuitry for the compensation of self-heating-induced timing errors, has been designed and fabricated in the IBM BiCMOS8HP process, utilizing 200 GHz f_T, trench-isolated, hetero-junction bipolar transistors (HBTs). Section 3 will discuss the design of this chip, in particular the self-heating compensation circuitry. In Section 4, the technique employed here for the assessment of the self-heating-induced timing errors experienced by a comparator circuit will be described. Finally, measurement results, validating the effectiveness of the self-heating compensation circuitry will be presented in Section 5, along with some interesting findings concerning the observed thermal behavior of the transistors on the comparator chip, and how that compared to the thermal behavior predicted by simulation.

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2. Self-heating effects and compensation

2.1. Self-heating in differential pairs

A common circuit building block of many high-performance comparator circuits, and the primary building block of the comparator presented here, is the differential pair amplifier. The primary mechanism by which self-heating affects differential pair amplifiers is temperature-dependent modulation of the transistors' base-emitter voltages. The transistor models utilized in the design kits of many IC processes account for self-heating effects by relating the local temperature rise of a device to power dissipation through a low-order thermal network for a given transistor, as described in [7,18]. Temperature-dependent device parameters vary according to the local device temperature determined by the self-heating model. Temperature-dependent base-emitter voltage modulation can be considered as an input-referred offset voltage, appearing in series with the differential pair input, as shown in Fig. 1. The temperature-dependent self-heating offset voltages are dependent on power dissipation of each transistor, and are therefore dependent on the amplifier's input signal. As signal-dependent offset voltages, in series with the input, the self-heating voltages provide a gain increase over the thermal bandwidth of the transistors, which is typically in the range of tens to hundreds of kilohertz. For a linear, broadband differential pair amplifier, the result, from a frequency-domain perspective, is a mid-band gain non-flatness, and, from a time-domain perspective, is a slow thermal tail in the step response. For a fully-switching, digital differential pair with a finite-slew-rate input signal, the result of the signal-dependent self-heating offset voltage is signal-dependent propagation delay variation. That is, a signal-dependent timing relationship between the input and output signal transitions that can be characterized as inter-symbol interference (ISI) or duty-cycle distortion (DCD).

A typical comparator circuit may consist of several cascaded differential pair gain stages, each of which may, depending on input signal amplitude, be operating in different regimes, varying from the linear regime to a fully-switching regime. Each differential pair gain stage may, therefore, experience the effects of self-heating differently. The design of a comparator circuit would ensure that, for even the smallest expected input signal, the output stage switches fully, in order to provide a digital output signal. Self-heating effects therefore manifest themselves at the output of the comparator as signal-dependent variation in the timing of the output signal switching instant relative to that of the input signal; this self-heating-induced timing variation can be characterized as DCD. In comparator applications where precise timing information is sought, self-heating poses a design challenge that must be addressed.

2.2. Self-heating compensation

Because the effect of self-heating in a differential pair can modeled as a signal-dependent, input-referred offset voltage, this effect can be eliminated by generating and feeding back a compensation signal to cancel the self-heating offset voltage. The feedback compensation scheme, illustrated by the block diagram of Fig. 2, utilizes a circuit block for the generation of the feedback compensation signal. The compensation signal generation block, shown in Fig. 3 is driven by a differential proportional-to-power (PTP) signal that is proportional to the differential power dissipation of the differential pair transistors. The PTP signal is applied to the collectors of transistors Q_1 and Q_2, thereby modulating their power dissipation proportionally to that of the transistors in the differential pair amplifier. Q_1 and Q_2 experience differential self-heating that is proportional to that of the amplifier transistors, and therefore experience base-emitter voltage modulation (i.e., a differential self-heating voltage) that is proportional to that of the amplifier transistors as well. This thermal voltage, appearing differentially between the Q_1 and Q_2 emitters, is amplified by a variable gain amplifier, whose gain is calibrated to

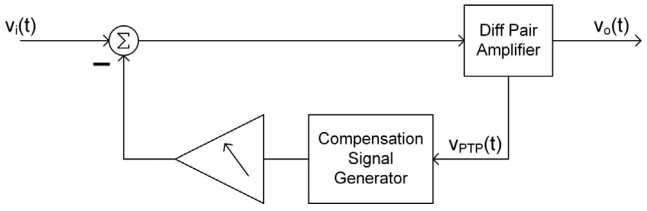

Fig. 2. Block diagram illustrating the feedback approach to self-heating compensation.

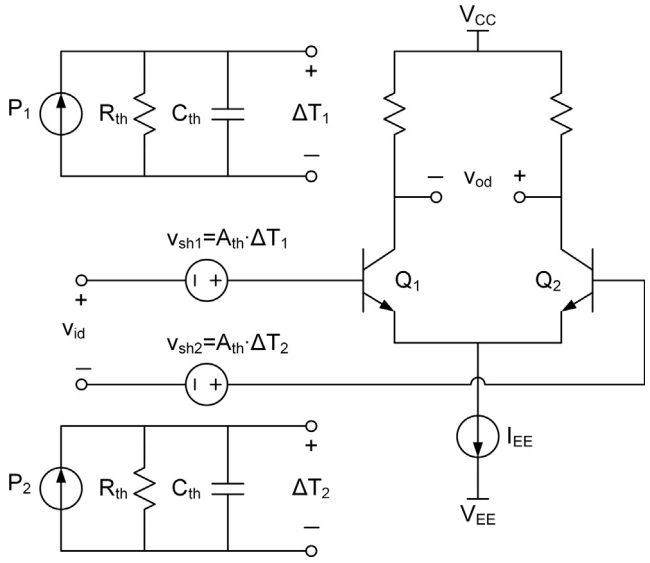

Fig. 1. Differential pair amplifier including self-heating-induced offset voltages.

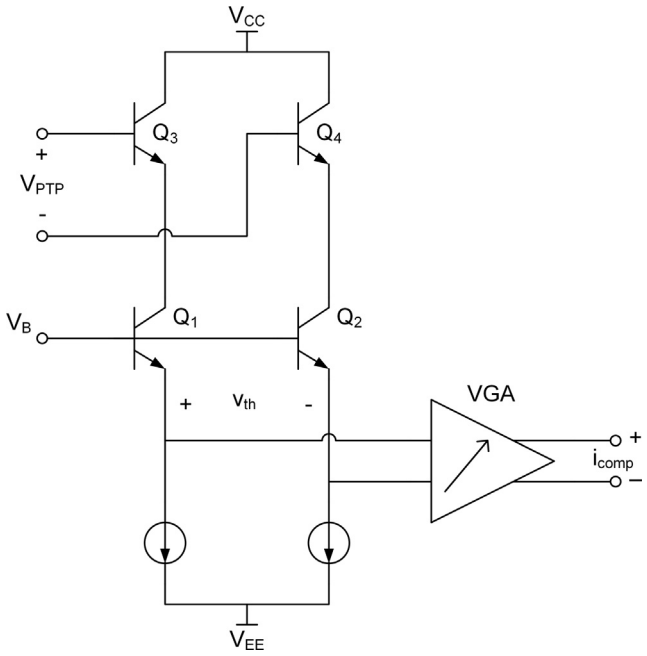

Fig. 3. Self-heating compensation signal generation circuit.