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Analysis and optimization of the two-stage pipelined SAR ADCs

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ABSTRACT

The two-stage pipelined SAR ADC (Successive Approximation Register Analog-to-Digital Convertor) is analyzed which consists of a SAR-based MDAC and a SAR ADC, with 1 bit redundancy to relax the requirement for the sub-ADC decision in accuracy. The stage resolution determines the performance of the ADC, which is optimized for high performance in linearity, noise, power, and speed. For the resolution of 10-bit, the optimal per stage resolution is about 5-bit in the first stage and 6-bit in the second stage. According to the analysis, a 10-bit two-stage pipelined SAR ADC was designed and fabricated in 180 nm CMOS, which achieves 56.04 dB SNDR and 5 mW power consumption from 1.8 V power supply at 50 MS/s.

1. Introduction

In recent years, low-power, moderate-resolution and moderate-speed ADCs are gathering attention in many electronic applications. Among them, pipeline ADCs have been widely used, but require several op-amps and numerous comparators, which result in large power dissipation [1]. Besides, SAR ADCs are favored due to their simple structure and high power efficiency [2,3]. However, the conversion speed of SAR ADCs is largely limited by their serial decision processes. Moreover, the area of SAR ADCs increases with the resolution, especially more than 10-bit. In many applications which require higher-performance ADCs, the above conventional structures (pipeline ADCs and SAR ADCs) could not meet the system requirement completely. As a result, new structures need to be innovated. Due to the perfect trade-off among speed, power, and linearity, the new structure of pipelined SAR ADCs has been widely researched, which is composed of pipeline ADC and SAR ADC [4–6].

In a pipeline ADC, larger first stage MDAC resolution improves the overall ADC linearity and relaxes noise and matching requirements, because the errors from the later stages are divided by the large inter-stage gain [5]. However, larger first stage MDAC resolution exponentially increases the area and power of the first stage MDAC because of the flash sub-ADC. Therefore, in the pipelined SAR structure, the flash sub-ADCs are replaced by SAR ADC, which makes the high-resolution MDAC possible. In addition, the sub-SAR ADC, which halves in resolution, also has a better performance in speed and area compared with a SAR ADC. Among the recent published pipelined SAR ADCs, Ref. [4] proposed a 12-bit 50 MS/s ADC using a typical two-stage pipelined SAR structure. Ref. [5] introduces 1.5-bit/cycle algorithm into the sub-SAR ADC to release the comparator offset constraint. And Ref. [6] presented a hybrid SAR-VCO ADC with a 5-bit SAR ADC as first stage and a VCO as second stage, which has considerable performance though oversampling.

Almost all papers on pipelined SAR ADCs employ two-stage structure, which pipelines a SAR-based MDAC with a SAR ADC generally. But many of those papers have not introduced how to optimize the per stage resolution in detail. Hence, this paper focuses on the basic principle of the two-stage pipelined SAR ADC and optimizes the stage resolution for a better performance in linearity, power, noise and speed. Finally, based on these basic principles and optimizations, a 10-bit two-stage pipelined SAR ADC was fabricated and measured.

The paper is organized as follows. Section 2 describes the proposed ADC architecture. Section 3 analyzes the impact of the stage resolution on the performance of ADC. The measurement results and discussion are shown in Section 4, followed by conclusions in Section 5.

2. ADC architecture

Fig. 1 shows the ADC architecture and timing diagram of the two-stage pipelined SAR ADC. It is comprised of a M_1-bit first-stage SAR ADC, a residue amplifier and a M_2-bit second-stage SAR ADC without a dedicated front-end S/H. Among them, the first-stage SAR ADC has a capacitive-DAC (CDAC) which also acts as the input sampling capacitor to reduce the area and to eliminate mismatch, while the conventional pipeline ADC has to use an

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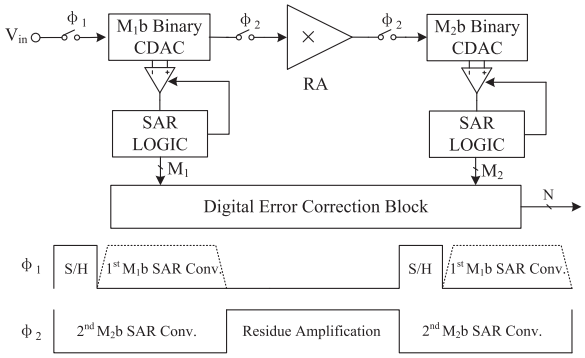

Fig. 1. Block diagram of the proposed ADC and its timing diagram.

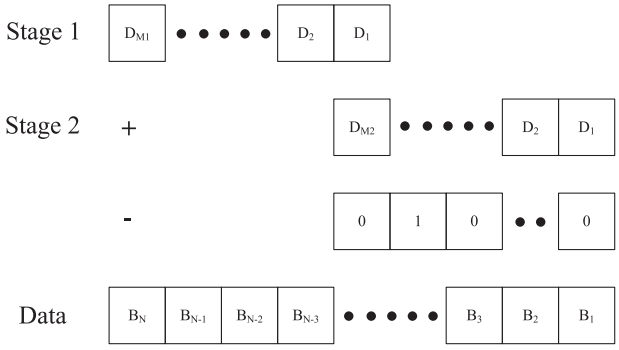

Fig. 2. Principle of the 1-bit redundancy digital error correction.

additional input sampling capacitor in the front-end S/H. As the proposed ADC works, the first stage SAR logic converts the coarse M_1-bit code and generates the residue on the top plate of the first stage CDAC, which is amplified by 2^{M_1-1} and sent to the second stage CDAC. And then, the second stage SAR ADC generates the M_2-bit fine code, when the first stage generates the next M_1-bit coarse code. Finally, these M_1-bit coarse codes and M_2-bit fine codes are combined together by the digital error correction logic in order to generate the final N (M_1+M_2-1) bits code.

In a conventional pipeline ADC, 0.5-bit redundancy is achieved by removing the top comparator in the flash sub-ADC, in order to eliminate comparing offset and to reduce power. However, in a pipelined SAR ADC, 0.5-bit redundancy is achieved by level shifting the signals which consumes extra time [5]. Therefore, for solving this problem of extra time, a simple 1-bit redundancy is used and the offset of $1/2^{M_1-1}V_{ref}$ from addition is eliminated by the digital correction, no longer by level shifting the residue signals, as shown in Fig. 2.

3. The impact of stage resolution on linearity, power, noise and speed

3.1. The impact of stage resolution on linearity

The ADC linearity depends on the first stage MDAC, because the next stage nonlinearity is divided by the stage gain. And the ADC nonlinearity mainly derives from capacitor mismatch and stage gain error, which can be reduced by employing large capacitor and high gain amplifier. Because the gain error is already discussed in the previous work, the capacitor mismatch is analyzed independently as follows.

The MDAC output can be expressed as

$$V_{MDAC} = (V_{in} - V_{DAC}) \cdot G \tag{1}$$

Ignoring the error of the stage gain G induced by the capacitor mismatch, the error of the MDAC output is

$$V_{MDAC\_error} = V_{DAC\_error} \cdot G \tag{2}$$

From (2), it can be seen that the MDAC nonlinearity is determined by the SAR-ADC nonlinearity, which has been discussed in [5,7]. Different from flash ADCs, the SAR-ADC nonlinearity varies with different SAR logics. For common analysis, by introducing a factor r, the nonlinearity of different SAR logics can be expressed as

$$\delta_{SAR} = \max(\delta_{dnl}, \delta_{inl}) = r \cdot 2^{-\frac{M_1}{2}} \frac{\sigma_u}{C_u} V_{ref} \tag{3}$$

where M_1 is the resolution of the first stage, C_u is the unit capacitor which is Gaussian random variable with standard deviation of σ_u. From [8], $r \approx 1$ in the conventional switching and $r \approx 1/\sqrt{2}$ in the V_{cm}-based switching. So the MDAC nonlinearity can be derived as

$$\delta_{MDAC} = \delta_{SAR} \cdot G = r \cdot 2^{-\frac{M_1}{2}} \frac{\sigma_u}{C_u} V_{ref} \cdot G \tag{4}$$

Note that the MDAC nonlinearity should satisfy the requirement for the resolution M_2 of the next stage and the resolution M_1 of the first stage sub-ADC, which can be given by

$$r \cdot 2^{-\frac{M_1}{2}} \frac{\sigma_u}{C_u} V_{ref} \cdot G < \frac{1}{2} \cdot \frac{1}{2^{M_2}} V_{ref} \tag{5}$$

$$r \cdot 2^{-\frac{M_1}{2}} \frac{\sigma_u}{C_u} V_{ref} < \frac{1}{2} \cdot \frac{1}{2^{M_1}} V_{ref} \tag{6}$$

Hence, the unit capacitor should satisfy that

$$\frac{\sigma_u}{C_u} < \frac{1}{r \cdot 2^{N+1-\frac{M_1}{2}}} \tag{7}$$

From (7), it can be seen that every 1-bit increase in M_1 relaxes the requirement for capacitor matching in the first stage by a factor of $\sqrt{2}$. Moreover, the larger the M_1, the larger the stage gain, which further divides the nonlinearity of the second stage.

To verify the previous analysis, behavioral simulations were performed which modeled the variation of the ADC nonlinearity when the first stage resolution M_1 changes from 4-bit to 7-bit in the 10-bit ADC. We assume that the first stage SAR ADC uses the V_{cm}-based switching, that the second stage uses the set and down switching, and that the two sub-SAR ADCs use the same unit capacitor. And we assume that the unit-capacitor values are Gaussian random variables with a standard deviation of $\sigma_u(\square C/C = 1\%)$, while the parasitic capacitance and gain error are not considered. As a result, the 1000-sample Monte Carlo simulation results are shown in Fig. 3, where the standard deviations of DNLs and INLs with respect to a best fit line are plotted versus the DAC input code at 10-bit level. As expected, the ADC nonlinearity decreases with the first stage resolution.

3.2. The impact of stage resolution on power

The power consumption of the ADC also varies with per stage resolution, and the power consumption of the ADC is mainly determined by that of the MDAC. Therefore, for simplicity, the power consumption of the first-stage MDAC is analyzed here to estimate that of the overall ADC. Note that this first-stage MDAC has an equivalent circuit diagram in Fig. 4, where C_1, C_2, and C_F are the equivalent load capacitances of the two stages determined by sub-SAR ADCs. For calculating C_1, C_2, and C_F, we assume that the unit sampling capacitors are C_{u1} and C_{u2} in the two stages, and that the parasitic capacitances of the amplifier and switches are