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Stacked field effect transistor integration in double channel transistors (DCT) with tri-state transfer slope and ballistic field effect behavior

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ABSTRACT

Implants create isolated electric charge under the channel region of nFET and pFET. By this, a new local extrema in the transfer slope is obtained while maintaining low leakage in off state. The results are explained by electro-static field simulation and yield in a circuit model with two parallel channel resistors, indicating a double channel field effect transistor (DCT). The new DCTs allow complex functions in logic or small transistor bit cells in the future.

1. Introduction

Because of the aggressive and very expensive pitch scaling in microelectronic technology, stacked and modified field effect transistor (FET) device integration is widely under discussion [1]. Improved FET devices with double or triple gate provide improvements by better control of short channel effects and with respect to performance [2,3], while multiple independent gate (MIG-) FETs [4] use an additional voltage biased gate electrode to dynamically modulate the sub-threshold swing. Dual channel devices enable negative differential channel resistance by using a two parallel device channel hetero structure [5] at expense of microelectronic technology costs. In [6] double channel nFET and pFET devices are demonstrated first time, implemented at low cost in standard 65 nm microelectronic device technology and applicable as static memory devices. In contrast to dual channel devices [5], double channel devices [6] have only one channel but acting dual, in enhancement or depletion mode, depending on applied body bias voltage [6]. This work demonstrates double channel devices manufactured in 45 nm silicon on insulator (SOI) technology and basic measurement results in floating body mode for improved device understanding and further application.

As presented in this work, double channel devices in floating body measurement mode have a negative transconductance region in the transfer slope also, reported so far from DCT measurements with forced body only [6]. This third state is a high resistance state at a gate voltage *VDCT* below threshold voltage and at low *VDS*, with a minimum leakage current even below *IOFF* at *VGS* = 0. This enables further development of DCT as memory devices in small transistor bit cells without body contact design and at low power consumption for large low voltage SRAM applications. Since in static memory cell application (SRAM) the maximum drive current in "on" state can be clearly reduced from high logic device FETs down to few μA, DCT are not necessarily high performance/high power devices. Because, the decoupled mechanism for minimum off-current and maximum on-current from threshold voltage (*Vth*) is a new property of DCT compared to FET devices, a further DCT device performance and technology optimization is promising. The DCT on-current was found initiated by the ballistic carrier transport effect in the output slope of the DCT devices, which might gain an DCT drive current (*IDS*) advantage in low power application compared to standard FET. Based on the measurement results a first order DCT SPICE model is presented in this work which suggests a circuit transistor model with two stacked parallel channels for further DCT circuit simulation.

2. Experiments

2.1. Technology of DCT manufacturing

As illustrated in Fig. 1a (process sequence order goes from top left to bottom right) a standard 45 nm CMOS technology on SOI substrates (88 nm silicon, 144 nm buried oxide on bulk silicon) was used to manufacture double channel devices. Prior the channel

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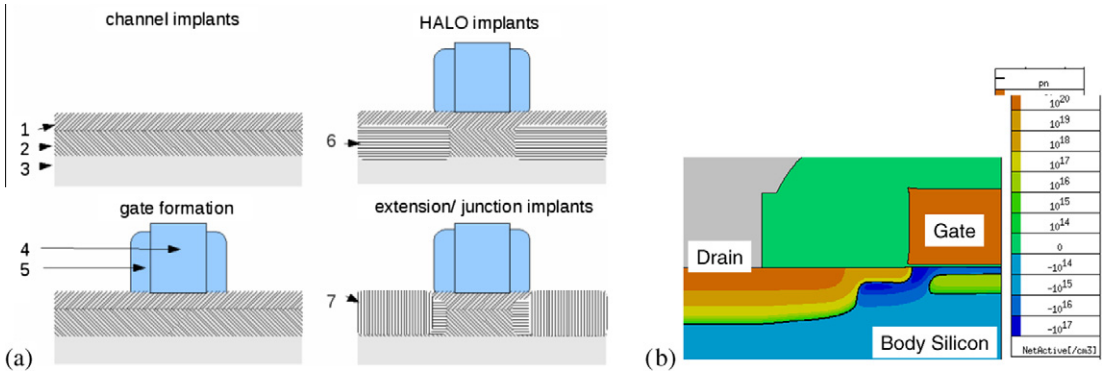

Fig. 1. (a) Schematic process flow of DCT device manufacturing in sequence from top left to bottom right. The numbers indicate: 1 – channel implant; 2 – double channel implant; 3 – silicon substrate; 4 – gate electrode; 5 – implant spacer; 6 – HALO implant; 7 – extension and junction implants. (b) Final sketch after source/drain implant and activation anneal out of the simulated double channel process flow to illustrate implant profiles and the location of the isolated dopant area under the gate electrode.

sub-threshold implant (1) one additional deep implant step (2), for n- and p-channel FET separate, was done into the surface silicon layer (3), pre-gate (4) and implant spacer (5) formation. This implant step (2) is called double channel transistor (DCT-) implant and forms a buried counter doped layer under the surface channel by using the same species and nearly the same implant energy and doses, as common for the post gate HALO implants (6) later in the process flow. The regular post gate pattering HALO implant (6) forms together with the DCT implant (2) a dopant island, isolated from junction implant area (7). In Fig. 1b a sketch of the simulated process flow after junction implant (7) and dopant activation anneal is shown. The isolated implant area under the surface channel affects the device transfer behavior electro-statically, by super positioning the gate potential and shortening the effective channel length for charge carrier transport along the drain-to-source path and depending on applied gate and drain voltage as discussed in following.

2.2. Electrical measurement results

The n- and p-DCT devices are measured in the lab at floating body and grounded source potential. As shown in Fig. 2 (left) DCT transfer slopes are measured at drain voltages (*VDD*) of 50 mV and 1 V as common for device characterization in linear and saturation mode and at 100 mV steps in between for further discussion. The measured output characteristics of DCT devices are shown in Fig. 2 also (right). From n- and p-DCT transfer slopes given in Fig. 2 the maximum drain-source-current *IDS*(*VDD* = 1 V) was measured of 190 μA/μm for nDCT and of −35.1 A/μm for pDCT. In linear mode (*VDD* = 50 mV) *IDS* is 23 μA/μm for nDCT and −8.3 μA/μm for pDCT. The *IOFF*(*VGS* = 0 V, *VDD* = 50 mV) is measured for nDCT at 4.7 pA/μm and for pDCT at-0.93 pA/μm. Maximum *IOFF*(*VGS* = 0 V, *VDD* = 1 V) is 2.5 nA/μm for nDCT and −8.2 nA for pDCT. For further characterization the linear and saturation trans-conductivities gm_{lin} and gm_{sat} are used as given in Eqs. (1) and (2)

$$gm_{lin} = \frac{\partial IDS}{\partial VGS}, \quad VDS = 50\ \text{mV} \tag{1}$$

$$gm_{sat} = \frac{\partial \sqrt{|IDS|}}{\partial VGS}, \quad VDS = 1\ \text{V} \tag{2}$$

The slopes for transconductance are shown in Fig. 3. Transconductance slopes are calculated by non linear function approximation analytical differentiation of the approximated graphs as described in [7] in order to avoid mathematical uncertainties of the local tangent method. Characteristic transconductance parameters of slopes in Fig. 3 are summarized in Table 1. To describe the DCT transfer slope, the gate-source voltage (*VGS*) at transconductance of zero ($gm_{lin} = 0$) is unique for double channel devices and labeled as *VDCT* therefore (see Table 1).

3. Discussion

3.1. Tri-state transfer slope of DCT

In Fig. 3a the DCT's transconductivity at 50 mV VDS is negative at zero gate voltage *VGS* and remains negative up to *VGS* = *VDCT* of around |0.17| V. The drain-source-current as a function of gate voltage, *IDS*(*VGS*, *VDS* = 50 mV), reaches a minimum at this point in Fig. 2. Beside *VGS* = 0 and *VGS* = 1 V, *VDCT* is a third state of DCT devices therefore. It is a low power and high channel resistance state, supporting the intended application of DCT devices in small transistor static memory cells [6]. The gate voltage *VGS* at $gm_{lin} = 0$ at *VDS* = 50 mV is called double channel threshold voltage *VDCT*. From transfer slope measurements shown in Fig. 2 it becomes obvious that the characteristic *VDCT* value diminishes above 200 mV of *VDS* for the given n- and p-DCT devices, which will be explained next. From general point of view, *VDCT* at low *VDS* only is not an issue with respect to the intended application of DCT for small transistor static bit cells, because in this case DCTs are required to act in non-inverter circuits, where low *VGS* is always correlated to low *VDS*. Furthermore, today's industry bit-cell stability is pushed towards low *VDD* values (actually 0.6 V and below) for general circuit applications with different sleep states, supporting DCT in tri-state transfer slope application. The stability of the VDCT state against electric noise is a concern, at least for the presented nDCT device transfer slope in Fig. 2, because the minimum *IDS*(*VGS* = *VDCT*) is just or even less than one order of magnitude below *IDS*(*VGS* = 0). Further DCT technology improvement will enhance the stability of the VDCT state against electric noise and exploratory research at DCT devices below 56 nm channel length is necessary. Another option to improve DCTs tri-state effect is the application in forced body mode circuits as illustrated in Ref. [6] first, but this is not subject of this work about basic DCT device properties.

To understand the double channel effect, that means the appearance of *VDCT* in the transfer slope of a FET, e.g., the effect of a buried charge under the gate on the electrical current flow between source and drain electrode, a simple superposition of coulomb fields from electro-static charges at drain *Q*(*Drain*) and gate *Q*(*Gate*) electrodes with and without a buried isolated charge *Q*(*buried*) is simulated in the arrangement shown in Fig. 4.

The simulation results are shown in Fig. 5, by the electro-static field *E* given in unit vectors and the electro-static field strength ϕ