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A technique to linearize the discrete-time parametric amplifier

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ABSTRACT

This paper presents a linearization technique to reduce harmonic distortion in a discrete-time parametric amplifier (DTPA). The technique may be applied to other variants of the DTPA, such as the complementary discrete-time parametric amplifier (CDTPA), the reverse discrete-time parametric amplifier (RDTPA), and the double-complementary discrete-time parametric amplifier (DCDTPA), to achieve similar, consistent, reductions in harmonic distortion. The parametric amplifier with and without the distortion-reducing linearization scheme was simulated for a standard 0.13 μm CMOS technology, with a sampling frequency of 250 MS/s and a 1.2 V power-supply voltage. The proposed technique shows 10 dB of mean reduction in the third-harmonic for a DTPA. Experimental results show a mean reduction in the third harmonic of 6 dB for a pMOS DTPA. The results exhibit consistent reduction in distortion for almost any input amplitude and any input common-mode voltage, without reduction in gain, without reduction in drive capability, and without any extra area requirement.

1. Introduction

A discrete-time parametric amplifier (DTPA) proposed in [1,2] samples and amplifies an input signal using a single MOS device. A DTPA uses MOS device properties to amplify an input signal using very little power and adding very low noise. A DTPA exhibits a common-mode voltage shift at the output terminal. To nullify this common-mode voltage shift [3,4] has proposed a complementary discrete-time parametric amplifier (CDTPA). In a CDTPA, an nMOS-DTPA and a pMOS-DTPA act as loads to each other. Yoshizawa and Lida [5] have proposed a gain-boosted double complementary discrete-time parametric amplifier (DCDTPA). The gain boosting in a DCDTPA is achieved through a reverse connected discrete-time parametric amplifier (RDTPA). [6] has proposed a low-power pipelined analog-to-digital converter using an RDTPA-based dynamic source-follower amplifier.

The DTPA, and all its variants, the CDTPA, the RDTPA and the DCDTPA, use basic MOS device properties to achieve amplification. The non-linearities of the MOS device properties create large harmonic distortion at the respective amplifier outputs. For example, in [2], a total harmonic distortion (THD) of −48 dB has been reported at 400 mV_{pp}, 1.4 V input common-mode voltage, and at a sampling rate of 100 kS/s. In the literature, the linearization techniques have been presented [7–10]. However, these techniques need extra circuitry. In this paper, the normal clocking scheme has been modified to linearize the DTPA and its variants.

The paper is organized as follows. Section 2 explains the working principle of a DTPA. In Section 3, a linearization technique is presented for the DTPA, and its role in harmonic distortion reduction is explained. Simulation results for a DTPA, using the proposed technique, are presented in Section 3.1. The paper is concluded with a performance summary in Section 5.

2. Parametric amplifier

2.1. Working principle of a DTPA

Fig. 1 [11] shows the cross sectional view of a single ended nMOS DTPA. The DTPA operates over three phases: track, hold and boost. In the track phase (Fig. 1(a)), ϕ_1 is high and ϕ_2 is low. The switch clocked by ϕ_1 turns on, and the source–drain (S–D) terminal of the nMOS transistor is connected to ground. The MOS capacitor is charged to a potential of $V_{IN}+v_{in}$. Provided the bias voltage, V_{IN} is greater than the threshold voltage of the device, the small-signal charge on the gate of the MOS capacitor is $C_{ox}v_{in}$, where C_{ox} is the oxide capacitance.

In the hold phase (Fig. 1(b)), the switches clocked by ϕ_1 and by ϕ_2 are open, while the S–D terminal of the nMOS transistor

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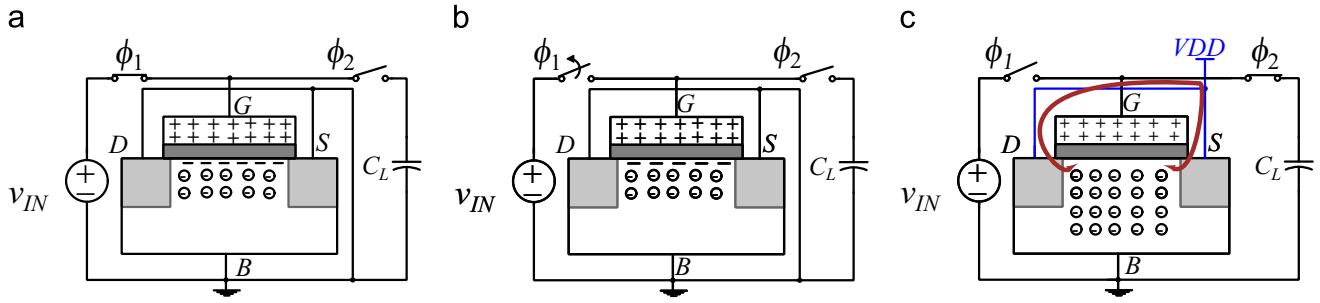

Fig. 1. Cross section of an nMOS DTPA in (a) track phase, (b) hold phase and (c) boost phase [11].

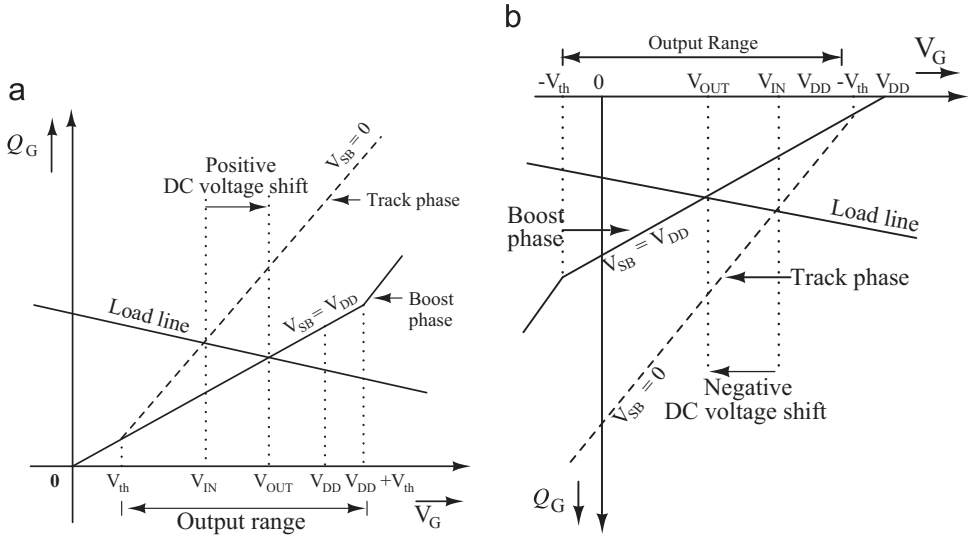

Fig. 2. Graphical analyses using Q_G–V_G relations for (a) the nMOS-DTPA, and (b) the pMOS-DTPA [3].

remains at ground. During the hold phase, the tracked input is held on the gate-terminal of the nMOS transistor.

In the boost phase (Fig. 1(c)), ϕ_1 is low and ϕ_2 is high. The input to the circuit is disconnected and now the gate is connected to the load capacitor, C_L. The S–D terminal of the nMOS transistor is connected to a large potential (V_{DD}). Assuming C_L is much smaller than C_{ox}, Q_G, the charge on the gate, remains almost unchanged from the hold phase. The mobile negative inversion charges available beneath the oxide layer are attracted to the large potential (V_{DD}) at the drain–source terminal. To compensate for the loss in inversion charge, the depletion charge in the body, Q_B, is forced to equal $-Q_G$. (The effective interface charge is neglected for simplicity.) The mean distance between the gate charge and the depletion charge is much larger than the oxide thickness, so gate-body capacitance is much lesser than C_{ox}. The charge held on the gate is almost the same as in the hold phase, the capacitance of the MOS device is much lesser than in the hold phase. Therefore the voltage at the gate of the transistor increases.

The sample phase of operation involves the sampling noise of $\frac{kT}{C}$. However, there is no resistors or active components are used when switching from the held phase to the boost phase. Hence, there are no noise sources involved in the amplification process after the sample and the hold phase. Therefore, the DTPA is ideally noiseless.

2.2. Graphical analysis

The action of a parametric amplifier is graphically analyzed in Fig. 2 [3] with the help of a load-line [12]. The charge on the gate of the MOS device approximately follows the dashed line during the track phase.

The intersection point of the dotted line (V_{IN}) and the dashed line ($V_{SB}=0$) marks the total charge on the gate at the end of the track phase. This charge is distributed to the load capacitance during the boost phase. The gate charge during the boost phase, $Q'_G(V_G)$, is given by the gate charge at the end of the track phase, Q_G, minus the charge on the load capacitance, $C_L V_{OUT}$. Accordingly, the load line has a slope of $-C_L$. The intersection point of the load line and the solid line marked as $V_{SB}=V_{DD}$ (the Q_G-V_G curve during the boost phase) gives the output voltage, V_{OUT}, during the boost phase.

The slope of the dashed line (during the track phase) is C_{ox}, whereas the slope of the solid line (during the boost phase) is C_{gb}. C_{gb} is the effective the gate to body capacitance when the transistor is in a weak-inversion mode. The ratio of C_{ox} to C_{gb} determines the gain of the parametric amplifier. The typical unloaded gain of a parametric amplifier varies between 5 and 10 depending on the fabrication process. For an nMOS DTPA, Fig. 2(a) shows bending in the slope of the boost phase line when V_G is more than $V_{DD}+V_{th}$. The nMOS DTPA changes the region of operation from the weak inversion to the strong inversion again when the gate voltage of an nMOS DTPA is more than $V_{DD}+V_{th}$. Similarly, the pMOS DTPA of Fig. 2(b) shows bending in the slope of the boost phase line[1] when V_G is less than $-V_{th}$. Hence, Fig. 2(a) and (b) shows that the output voltage range of both pMOS-based and nMOS-based DTPAs is V_{DD}. An nMOS-DTPA (Fig. 2(a)) shows a positive DC voltage shift while a pMOS-DTPA shows a negative average voltage shift (Fig. 2(b)). This limits the use of nMOS or pMOS based DTPAs in applications requiring a cascade of stages.

[1] The DTPA changes the region of operation from a weak- to a strong-inversion mode.