Microelectronics Journal 46 (2015) 1082–1090

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Impact of lateral straggle on analog and digital circuit performance using independently driven underlap DG-MOSFET

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ARTICLE INFO

Article history:
Received 11 October 2014
Received in revised form
12 May 2015
Accepted 26 August 2015
Available online 26 September 2015

Keywords:
Symmetric DGMOS
Lateral straggle
Variable gain amplifier
Amplitude Modulator
Modulation index
Efficiency
SRAM
Static Noise Margin

ABSTRACT

In this work, the effect of lateral straggle on independently driven underlap double gate MOSFET (IDUDGMOS) is presented based on analog and digital circuit performances. The lateral straggle in IDUDGMOS devices is due to process induced source/drain out diffusion and it varies the desired device characteristics. For the analysis of this variation on circuit performance of the device, an Amplitude Modulator (AM) circuit and a SRAM circuit is considered for analog and digital circuit application considerations respectively. For the analysis of the device in AM circuit the parameters studied are the bandwidth, the gain and the linearity, correspondingly for SRAM circuit the parameters studied are the Static Noise Margin (SNM) and the circuit delay. The analysis of the AM circuit designed using the IDUDGMOS suggested that the power loss and the bandwidth of the circuit degrade with increasing lateral straggle. For the SRAM circuit the analysis suggests that larger straggle lengths in the device results in reduced time delay but, the SNM is smaller as well.

1. Introduction

With an advancement of the mobile and handheld technology, the needs of low power analog and digital circuit are growing each day. In the communication domain, low power on chip modulators are in high demand [1] whereas from the perspective of a digital designer a low power SRAM will be handy in designing memory component for low power handheld devices like tablet PC, Smart Phones and Satellite Phones. Now a day the mobile communication is working in the bandwidth of 900 MHz to 5 GHz which includes the Global System for Mobile (GSM), Code Division Multiple Access System (CDMA) and Wi-Fi. As a result low power on chip modulator with a bandwidth of 900 MHz to 5 GHz will be good building block for today's mobile systems. With the advancement of microelectronics technology, followed by Moore's Law, the size of transistor is reducing every year resulting a real challenge in the design of a modulator in the decananometer regime with controlled short channel effect (SCE).Whereas for the storage technology it is hard to design a SRAM with high SNM for a supply voltage of 1 V. At the same time it is hard to reduce the access delay of the SRAM. Both the SNM and delay are controlled by the SCE for a decananometer device. The IDUDGMOS can be a very good alternative [2,3] in designing all the foresaid circuit as two gates of the device offers better control over the channel [4] which provides lowered SCE and higher on current (I_{on}) to off current (I_{off}) ratio where I_{on} is the on current at drain bias, V_{DD}= 1 V and I_{off} is the off current at V_{gs}=0 and V_{DD}= 1 V. The I_{on}/I_{off} is optimized for the source underlap length and drain underlap length as in [4]. The IDUDGMOS also provides few more advantages. It is found that higher V_T gives higher SNM. As the IDUDGMOS is having relatively higher V_T for lower supply voltage it can be a very good alternative for low power SRAM design. At the same time due to the Independent gate property of IDUDGMOS the transconductance can be modulated by the back gate voltage [4]. Also the IDUDGMOS provide a high bandwidth which will be useful to design a wideband modulator. All the factors like V_T and transconductance of IDUDGMOS are dependent on process dependent parameter lateral straggle due to source drain out diffusion [5]. Lateral straggle is the maximum distance where the Source/Drain concentration goes below the channel doping concentration value. The variation of straggle length (L_S) causes a change in the effective channel length which results in variation in Analog/RF performance of the circuit [5]. At the same time L_S controls the V_T of the device [5]. As a result SNM of a SRAM can be controlled by changing the L_S of IDUDGMOS and gain-bandwidth can also be controlled by changing the L_S. In this work, effect of L_S of the IDUDGMOS device in Amplitude Modulator and SRAM is observed. In earlier work a 200 MHz bandwidth Modulator circuit designed using VGA based on CMOS technology has been reported [6]. An AM circuit with lesser transistor count using the

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http://dx.doi.org/10.1016/j.mejo.2015.08.011
0026-2692/

IDUDGMOS devices is designed in this work. Few previous work [7] report a SRAM designed in DGMOS with write delay of 8.97psec and Write Static Noise Margin(WSNM) of 0.505 V. In this work a SRAM with 6 transistor(6T) architecture and improved SNM and delay performance over existing circuit [7] is presented.

2. Device structures

In this work, effect of lateral straggle on analog and digital circuit performance are observed considering AM circuit and SRAM circuit as reference for three straggle length of IDUDGMOS. The IDUDGMOS device structures are shown in Fig. 1. These devices are later used to design and analyzed the performance of an AM & SRAM circuit. 2D numerical simulator [8] is used to perform all the simulations using Density Gradient carrier transport model.

In the IDUDGMOS structure under consideration, the source/drain underlap length and the front/back gate oxide thickness are equal. All the devices parameters are considered according to the International Technology Roadmap for Semiconductors (ITRS) for 45 nm gate length devices [9]. IDUDGMOS device having a gate length (L_G) of 45 nm, channel thickness (T_{si}) of 16 nm and gate height (T_g) of 10 nm. Molybdenum is used as gate material with work function of 4.52. Front/Back oxide thickness is 1.9 nm. Drain/Source Underlap length is 20 nm channel doping concentration of 10^{15} cm^{-3} is considered. A Gaussian like profile which is described by the equation.

$$N_{sd}(x) = N_{peak} exp\left(-x^2/L_S^2\right) \quad (1)$$

where x is the position from source/drain (S/D) into the channel, N_{sd} signifies the doping concentration at point x. N_{peak} is the maximum S/D doping concentration, L_S is lateral straggle length [10], is implemented for Source Drain lateral Straggle Doping profile. Three different straggle lengths (L_S) of 3 nm, 5 nm and 7 nm are considered in this work for study. Fig. 2 shows the simulated doping profile of three different L_S of IDUDGMOS.

During the simulation, Aurora mobility model is used which includes ionized impurity scattering and temperature dependency [11]. Active carrier lifetime and density are modeled using Shockley–Read–Hall (SRH) recombination and for carrier transport drift diffusion model is considering. For the generation of robust simulation structure, meshing strategy presented in [12] is used. The standard experimental data considering the carrier mobility as a function of inversion charge [13] is used to calibrate the simulator. The on current (I_{on}) to the off current (I_{off}) ratio [3] optimization of the underlap length for the device structures are done. All the circuits are biased at 1 V of supply voltage. In next section, the design and analysis of the AM circuits and SRAM is carried out using the three different L_S IDUDGMOS.

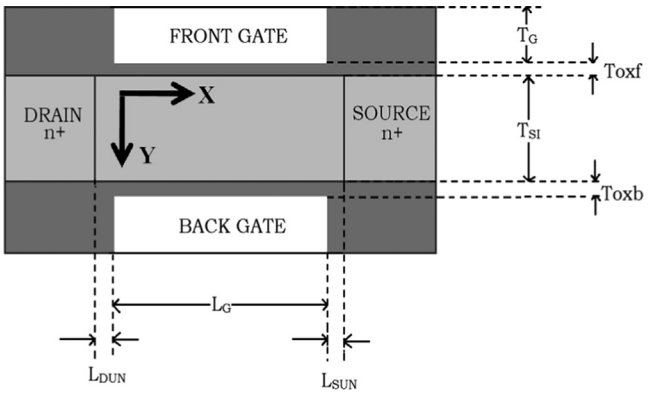

Fig. 1. IDUDGMOS Device structure.

3. Analog & digital performance

In this section, effect of lateral straggle of IDUDGMOS in analog and digital circuit performance is observed. The whole section is divided into two parts. In the first part effect of lateral straggle in Analog performance is observed using an AM circuit which is followed by the study of SRAM for the digital performance study.

4. Analog performance study

In a conventional AM circuit the modulated voltage is the product of message signal and the carrier signal [14].The expression of the Amplitude Modulated signal is represented as $x(t) = m(t) \times c(t)$, where $m(t)$ and $c(t)$ are the message and carrier signal respectively.

To design an AM modulator the main target is to design a multiplier. In a conventional differential amplifier the output gain is dependent on the current of the lower most MOSFET namely tail MOSFET, MN3 in Fig. 3. The gain expression for the double ended differential amplifier, is given by [15].

$$A_v = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{ss}} \cdot R_D \quad (2)$$

where, A_v=Gain of the differential Amplifier, μ_n = mobility, C_{ox}=Gate oxide capacitance, W/L=aspect ratio of the n-channel MOSFET (nMOSFET), R_D= load resistance and I_{ss} is the drain current of the tail MOSFET. From Eq. (1) it is evident that, if the tail MOSFET is in saturation then the I_{ss} will be solely dependent on the gate voltage. Output voltage of a circuit V_O is represented as $V_O = A_V \times V_{IN}$where A_V is the voltage gain and V_{IN} is the input

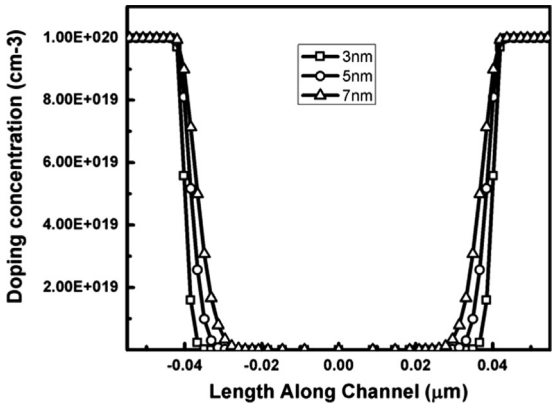

Fig. 2. Doping concentration for various straggle length as a function of channel length.

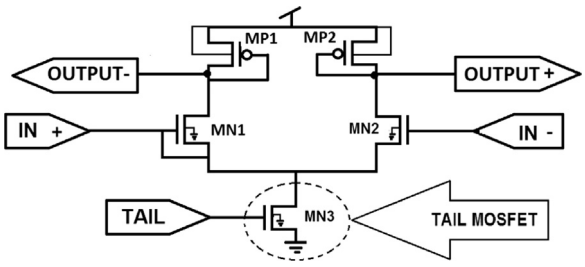

Fig. 3. Differential amplifier with encircled tail MOSFET.