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Effect of a surface pre-treatment on graphene growth using a SiC substrate

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ABSTRACT

This study reports surface pre-treatment techniques for the formation of a high-quality graphene layer on a SiC surface. It is demonstrated that silicon passivation of SiC surface using a silane flow and subsequent sacrificial oxidation can significantly improve the surface condition of a graphene layer on SiC by ensuring much fewer carbon dumps and wrinkles, reducing the electrical resistance, and providing smoother surface roughness and a larger domain size. The effect of in situ cleaning by a SF_6 treatment before graphitization was also studied. It was found that in situ cleaning using SF_6 gas can be a simple and effective means of improving the quality of a graphene layer grown on SiC. The results of this study suggest that a surface treatment before graphitization is the key to synthesize high-quality epitaxial graphene layer.

1. Introduction

Graphene has attracted a great deal of attention as a promising candidate material for future electronic devices due to fascinating electrical properties such as its ballistic transport of electrons [1–3]. To realize graphene electronic devices, it is necessary to develop a process for the synthesis of graphene on a large scale. Among the reported methods of synthesizing graphene, epitaxial growth on a SiC substrate by silicon sublimation can be an effective means of producing a large-scale graphene layer [4]. However, there is usually a large amount of carbon agglomeration and wrinkles on the surface of graphene that is epitaxially grown on SiC. Though several hypotheses have been suggested regarding the origin of such carbon defects, no experimental confirmation has been reported thus far [5]. This study shows that SiC surface preparation before graphitization is a critical factor for achieving a high-quality graphene layer. Additionally, new methods to improve the quality of graphene on SiC by both the ex situ and in situ cleaning of the SiC surface are proposed and demonstrated. Ex situ cleaning uses a silane pre-treatment on the SiC surface which is followed by sacrificial oxidation. In situ cleaning uses annealing in a sulfur hexafluoride (SF_6) gas ambient prior to graphitization.

2. Experimental

All of the SiC wafers used for the experiment were chemical mechanical polished (CMP) epi-ready, Si-terminated *n*-type 4H-SiC (0001) on-axis single crystal wafers with a resistivity of 0.013–0.5 Ω cm. They were obtained from Cree Inc. Graphene layers were epitaxially grown on the surfaces of the SiC wafers in a high vacuum furnace with a vacuum level of $2–5 \times 10^{-6}$ Torr at 1430–1450 °C for 5–10 min. The heating rate was approximately 50 °C/min. Before loading then into the furnace, all of the SiC wafers were cleaned by piranha cleaning (1:1 = H_2SO_4:H_2O at 150 °C) for 10 min and subsequently dipped into a diluted HF solution (1:10 = HF:H_2O) for 1 min. Selected samples were put through a silane pre-treatment, sacrificial oxidation or in situ cleaning via a SF_6 treatment. These processes are discussed later in this paper.

3. Results and discussion

3.1. Effect of native oxide on the growth of graphene

Fig. 1 shows the root mean square (rms) surface roughness of graphene epitaxially grown on SiC at 1430 °C for 10 min after the chemical cleaning processes mentioned above. The rms roughness was measured using AFM, scanning over an area of $2 \times 2\ \mu m^2$. It is interesting to note that the time to reach to the high vacuum state after sample loading significantly affects the quality of the graphene in terms of the surface roughness. When the time duration of pumping down is 6–13 min, the rms roughness is in the range of 2.5–3 Å. However, when the pumping down exceeds 20 min,

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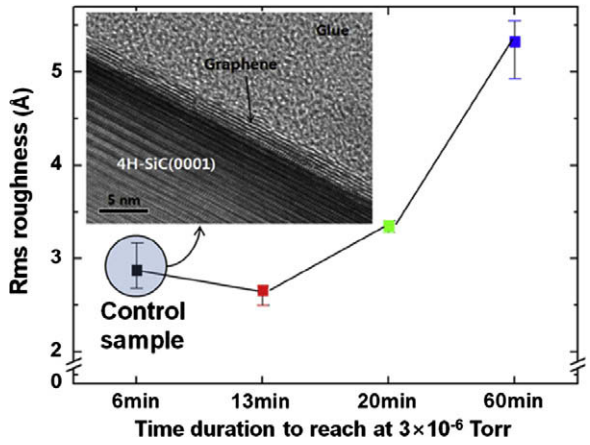

Fig. 1. The rms roughness of graphene layers with respect to the pumping down time to reach a vacuum level of 3×10^{-6} Torr. Graphitization was done at 1430° for 10 min. Inset: TEM image of a graphene layer when the pumping down time is 6 min.

the rms roughness increases significantly. This suggests that the amount of native oxide on SiC grown by the reaction with the residual oxygen in the chamber before reaching the high vacuum is an important factor for uniform graphitization. A transmission electron microscope (TEM) image is shown in the inset of Fig. 1 of a sample for which the pumping down time was 6 min, which is the shortest time achievable in our system. The TEM result shows that a few graphene layers appear to have grown well on the SiC surface. However, it should be noted that TEM reveals only a very small area of the sample. When a STM image of the same sample over an area of 100×100 nm^2 is examined, a large amount of carbon agglomeration can be observed, as shown in Fig. 3(a), despite the fact that the sample has the shortest pumping down time of 6 min. This highlights the necessity of the surface treatment of the SiC surface in the vacuum chamber, which effectively removes the native oxide prior to graphitization.

3.2. Surface passivation using silane for the epitaxial growth of graphene

As it has been reported that Si atom flux on a SiC surface can help dissolve the native oxide on SiC during graphitization [6], a new method using silane pre-treatment is proposed. The silane pre-treatment process is a conventional silicon process style method which is suitable for large-scale wafer processing and high-volume production. In the experiment, silane pre-treatment was performed on a SiC wafer surface prior to the loading of the SiC wafer into the graphitization chamber. It was done at 400 °C at a pressure of 2.4 Torr with a silane (SiH_4) gas flow rate of 300 sccm for a time duration ranging from 30 s to 5 min. Through this silane treatment, the SiC surface is passivated with a monolayer or a few layers of silicon. For graphitization, the SiC wafers were thermally decomposed at 1450 °C for 5 min in the chamber.

As agglomerated carbon dumps and wrinkles on the surface of the graphene layer affect its electronic properties [7], electrical resistance measurement on graphene surface can serve as a quick monitoring tool to evaluate the quality of a graphene layer grown on SiC. Fig. 3(a) shows the change of the electrical resistance of graphene layers grown after a silane pre-treatment with various time durations. The electrical resistance of the samples is measured on the graphene surface by probing two locations of the graphene layer using a probe station and a semiconductor parameter analyzer, as shown in the inset image in Fig. 2(a). The distance between the two probe tips on the sample is fixed at 11 mm. The results show that all samples with the silane pre-treatment exhibit much lower resistance compared to the control sample, indicating that silicon passivation using a pre-silane treatment prior to graphitization improves the surface quality of graphene layers. A silane pre-treatment duration of 1–2 min appears to be the optimum condition. The resistance increases again when the silane pre-treatment time is 5 min. This is most likely due to excess silicon on the surface, which may block Si sublimation from SiC. In further experiments, therefore, the time duration of the silane treatment was fixed at 1 min. In an attempt to improvement of the surface property even more, a sacrificial oxidation technique prior to graphitization was employed, in an analogy to the gate oxidation pre-treatment in the CMOS process. The sacrificial oxidation was done chemically using a boiled H_2O_2 solution for 20 min. Fig. 2(b) shows the thickness of SiO_2 grown on the surface of silane-treated SiC wafers during the sacrificial oxidation process. The oxide thickness increases with the silane treatment time but eventually becomes saturated after 1 min of silane treatment. This result confirms again that a time of 1 min is sufficient for silicon passivation on a SiC surface.

Fig. 3 exhibits STM images taken using a constant-current mode at room temperature. The control sample in Fig. 3(a) after only

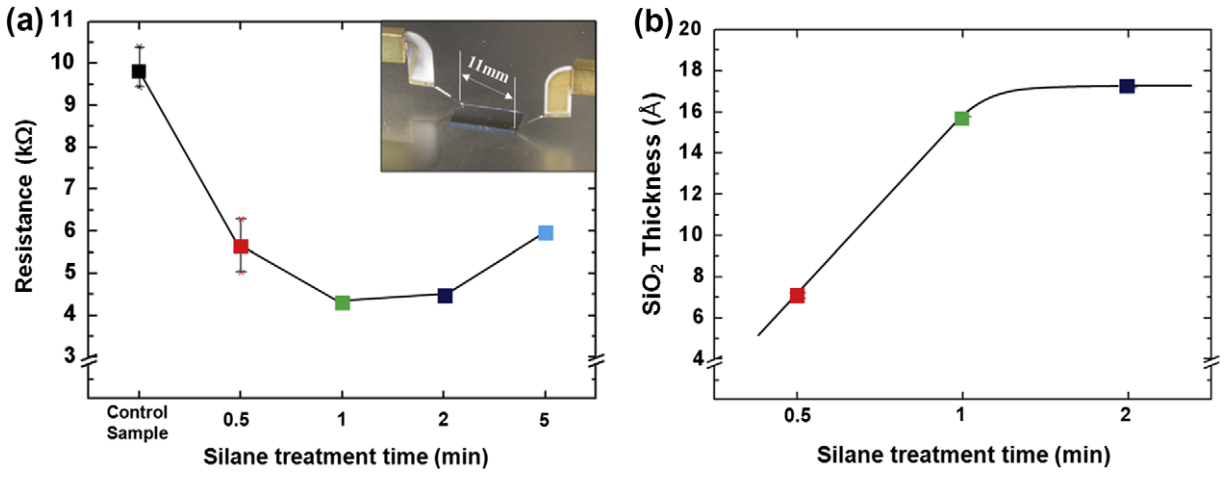

Fig. 2. (a) The electrical resistance of epitaxially grown graphene samples after a silane pre-treatment with various silane treatment times. The resistance was measured by probing two locations of the graphene layers with a fixed distance of 11 mm (see the inset image). (b) The thickness of SiO_2, grown by sacrificial oxidation, on the surface of silane-treated SiC wafers with different silane treatment times.