Microelectronic Engineering 87 (2010) 2014–2018

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Effects of nitrogen incorporation by plasma immersion ion implantation on electrical characteristics of high-*k* gated MOS devices

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ARTICLE INFO

Article history:
Received 9 August 2009
Received in revised form 18 November 2009
Accepted 21 December 2009
Available online 4 January 2010

Keywords:
High-*k* gate dielectric
HfOxNy
Nitridation treatment
Plasma immersion ion implantation

ABSTRACT

Nitridation treatments are generally used to enhance the thermal stability and reliability of high-*k* dielectric. It is observed in this work that, the electrical characteristics of high-*k* gated MOS devices can be significantly improved by a nitridation treatment using plasma immersion ion implantation (PIII). Equivalent oxide thickness, (EOT) and interface trap density of MOS devices are reduced by a proper PIII treatment. At an identical EOT, the leakage current of devices with PIII nitridation can be reduced by about three orders of magnitude. The optimal process conditions for PIII treatment include nitrogen incorporation through metal gate, ion energy of 2.5 keV, and implantation time of 15 min.

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1. Introduction

As the gate oxide thickness of MOS devices becomes thinner with the scaling down of semiconductor devices, higher gate leakage current occurs. One method for increasing gate capacitance, thus, limiting the leakage, is to increase dielectric constant by replacing SiO_2 with a high-*k* material. A thicker gate dielectric cannot only reduce the leakage current flowing through the structure but also improve the reliability. Therefore, high-*k* gate dielectrics have been proposed to replace SiO_2 for nano-scale MOS device applications [1]. Although it can reduce gate leakage current, the interface quality of high-*k* material with silicon is a critical issue. Usually, the interface property can be improved by some kinds of nitridation treatment, but nitrogen atoms often diffuse to Si substrate surface after nitridation treatment. The NO_x related fixed oxide charge near the gate oxide/Si interface would cause column scatter and mobility degradation. NH_3, NO and N_2O are generally applied for thermal nitridation. However, it is not easy to incorporate enough nitrogen into high-*k* dielectric by using a thermal nitridation treatment. To incorporate more nitrogen into dielectric, a high temperature process is applied in current nitridation treatment, which would increase EOT due to the formation of low-*k* interfacial layer. Proper nitridation can effectively suppress the diffusion of impurity into gate dielectric and decrease the interfacial oxide formation from the out-diffusion of oxygen in Si substrate [2]. Recently, plasma immersion ion implantation (PIII) is becoming a favorable technique for dopant incorporation [3,4]. The sample to be treated by PIII is placed in a vacuum chamber where RF of microwave plasmas are created containing ions of the species to be implanted. Repetitive, high negative-voltage pulses ranging from 2 to 300 kV are then applied to the sample, causing ions to accelerate through the sheath [5]. PIII possesses has several advantages such as high-dose, shallow depth, low damage, and precise depth. Although the effects of nitrogen incorporation into hafnium oxide by PIII on physical characteristics of high-*k* gated MOS devices were studied [6], its electrical characteristics are rarely reported. In this work, the effects of various PIII nitridation treatments on the electrical characteristics of high-*k* gated MOS devices are studied.

2. Experiment

MOS capacitors with TaN/HfOxNy/Si structures were fabricated on a (1 0 0)-oriented 6-in *P*-type Si wafer with resistivity of 15–25 Ω cm. After RCA clean, the HfxNy (~2.0 nm) gate dielectric was deposited by a reactive dc magnetron sputtering (Ion Tech Microvac 450CB) with a 99.99% pure Hf target in Ar/N_2 = 24/36 sccm at power = 100 W and pressure = 7.6 mTorr. Then, a post deposition annealing (PDA) at 850 °C in N_2 gas for 30 s was performed to form HfON. Subsequently, a 50 nm thick TaN film was deposited by sputtering (ULVAC Sputter SBH-3308RDE) to serve as the metal gate, at pressure = 6 mTorr and power = 500 W. After metal gate deposition, PIII nitridation was applied. In this work, the ion were performed at 1.5–40 keV with various operation time

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doi:10.1016/j.mee.2009.12.082

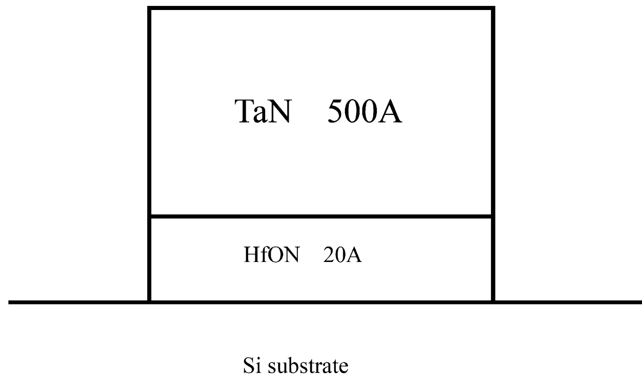

Fig. 1. Schematic cross-section of MOS device in this work.

ranging from 5 to 15 min in N_2 = 84 sccm at RF power = 300 W and pressure = 0.6 mTorr. For 10 min implantation, the dose is about 5×10^{13}. An annealing treatment was performed at 850 °C after the PIII. Then, a post metal annealing (PMA) was carried out at 850 °C in N_2 gas. After a 300 nm Al deposition, the Al/TaN was patterned by a helicon-wave plasma etching (Anelva ILD-4100) in Cl_2 90 sccm and N_2 10 sccm at RF power = 1900 W and bias power = 120 V. A 500 nm thick Al film was then deposited on the backside of all samples. Finally, a sintering was conducted in a N_2/H_2 ambient at 450 °C for 30 min. Fig. 1 shows the structure of the MOS device.

3. Results and discussion

3.1. Effects of PIII on the electrical properties of high-k gated MOS device

Fig. 2a shows the leakage current density (J_g) and EOT for high-*k* gated MOS devices with various PIII nitridation treatments. The error bars were obtained by taking about 20 samples for statistic analysis, which indicates the uniformity of devices with various treatments. The leakage current density for samples with PIII nitridation is clearly lower than that without it. This reduction in leakage current may be explained as that most of N atoms are located in the upper layer of dielectric. For the sample with PIII at lower ion energy, Hf–N bonds are formed in dielectric bulk; large amount of Hf–N can suppress the diffusion of impurity in gate dielectric and the interface trap generation of Hf–O–Si [7]. For samples treated by PIII at ion energies of 2.5–10 keV, the EOT has reduced and the leakage current has decreased by about three

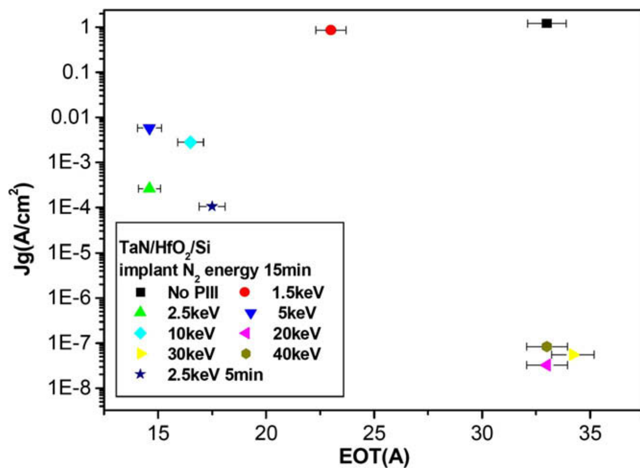

Fig. 2. Leakage current density and EOT for devices with various PIII nitridation.

orders of magnitude in comparison with that without PIII. The EOT value of the sample with PIII nitridation at ion energy of 1.5 keV is larger than that of 2.5 keV. Ion energy of 1.5 keV is not enough to result in an adequate incorporation of N into dielectric, some N atoms are still incorporated in the metal gate.

The *C–V* curves for high-*k* gated MOS devices with PIII nitridation at (a) 2.5, (b) 5 and (c) 10 keV are depicted in Fig. 3. The EOT and flat-band voltage (*V*fb) were extracted from a simulation program considering quantum effect [8]. Because the simulated *C–V* curves are obtained from MOS device with ideal high-*k*/Si interface, the distortion of *C–V* curves during the accumulation-to-inversion transition in Fig. 3b and c indicates the existence of some interface traps at high-*k*/Si. For the sample with PIII at 2.5 keV, an EOT value of ~1.45 nm is achieved and its interface trap density (Dit) is about 10^{11} cm^{-2} eV^{-1}, which is lower than normal cases (5×10^{11}–10^{12} cm^{-2} eV^{-1}). The low Dit is caused by the good SiON layer formed on Si substrate. In Fig. 3, the depth of the nitrogen implantation for the sample with PIII at 2.5 keV is at high-*k*/metal gate, and those at 5–10 keV is at high-*k*/Si substrate or inside Si substrate.

Fig. 4a shows hysteresis-induced flat-band voltage shifts (ΔVfb) of MOS devices with various PIII nitridation at ion energies of 20–40 keV. As implantation energy increases, the ΔVfb values become larger. Fig. 4b shows ΔVfb of MOS devices with various PIII nitridation at ion energies of 1.5–10 keV. The hysteresis for samples with PIII nitridation is slightly larger than those without, especially for those with more nitrogen incorporation. These results may be due to the existence of N-related traps in the high-*k* dielectric [9]. For the case of ion energy of 2.5 keV in PIII, the hysteresis of sample with implantation time of 5 min is two times larger than that of 15 min, because a low concentration of nitrogen dopant is not enough to suppress the diffusion of impurity in gate dielectric.

The electrical characteristics of MOS devices may be affected by several ways for nitrogen incorporation. Thus, nitridation on Si surface, through gate electrode, through sacrificial oxide and through metal gate were preformed for 15 min implantation time; the resulting electrical properties of MOS devices were compared. The conductance (G_p) as a function of frequency (ω) were measured and plotted as $G_p/\omega A$ versus by biasing the Si surface in depletion condition to study the interface properties. Fig. 5a shows EOT and J_g with different ways of PIII nitrogen incorporation. The sample with nitridation through metal gate and 5 min implantation shows the lowest leakage current but higher EOT; this may be due to the fact that only few N atoms are located in the high-*k* dielectric. For the sample with 15 min implantation and 2.5 keV ion energy, the leakage current and the EOT both decrease; this optimal results attributed to the litter damage and suitable nitridation incorporation. Fig. 5b shows Dit of MOS devices with different ways of PIII nitrogen incorporation at 5 min. The sample with implantation from top gate has the lowest Dit.

3.2. The reliability characteristics of high-k gated MOS devices with various PIII nitridation treatments

Fig. 6 shows the stress-induced flat-band voltage shift (ΔVfb) of MOS devices as a function of stress time under a constant electrical field stress of −14 MV/cm. The stress-induced ΔVfb for samples with PIII nitridation at high energies is larger than that at low energies, because high energy implantation would induce oxide trap in high-*k* dielectric. Since bulk traps in dielectric are induced by implantation damage, the stress-induced ΔVfb for samples with PIII at low energy are still slightly larger than that without PIII nitridation. Fig. 7 shows the stress-induced leakage current (SILC) of MOS devices as a function of stress time under a constant electrical field stress of −14 MV/cm. SILC value for sample with PIII nitridation at a high energy is larger, because high implantation

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