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A new controllable adaptive biasing linearization technique for a CMOS OTA and its application to tunable Gm-C filter design

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ABSTRACT

This paper presents a new linearized operational transconductance amplifier which uses a fully controlled adaptive biasing scheme. The differential input voltage is sensed through a squarer circuit and is compared with a controllable reference voltage to create appropriate auxiliary tail currents. The proposed adaptive biasing circuit can be adjusted to make best linearization for each tuning condition of OTA. While the adaptive biasing circuit consumes a little portion (about 13%) of the total power consumption (about 475 μW), it significantly reduces the third-order nonlinearity of OTA's output current in whole of its tuning ranges. By applying a two-tone 0.6 Vp-p input voltage at 20 MHz, IM3 is degraded by more than 13 dB throughout the transconductance tuning range from 8.2 μA/V to 47 μA/V. Proposed OTA is employed to implement a wide tunable Gm-C filter. The cutoff frequency of low-pass filter is tunable from 584 kHz to 10.6 MHz, thus, it covers several standards of wireless applications. IIP3 of filter is 22.3 dBm, 19 dBm and 17.4 dBm, respectively, for Bluetooth, UMTS and IEEE 802.11a/g standards. The OTA and Gm-C filter are designed and simulated in 0.18-μm TSMC CMOS technology with Hspice simulator. Monte Carlo and corner case simulations show the good robustness of proposed circuits against the fabrication errors.

1. Introduction

Recent trend in wireless and wireline communication systems is portable multi-standard receivers with the highest level of integration and ability of support new services by minimum hardware addition [1–4]. Hence, direct conversion receivers with most integration capability and design of tunable circuits as building blocks have been interested in recent research [5–9].

Channel select filter as one of the main building blocks in the analog front-end part of receivers is responsible for selecting desired channel, blocking interferes, and providing anti-alias filtering before the subsequent analog to digital conversion stage. In the case of multi-standard receivers, channel select filter needs wide frequency tuning range and high selectivity with respect to desired channels [10,11].

Transconductor (Gm)-C, active-RC and MOSFET-C structures are the main solutions for implementation of analog channel select filters. Among them, Gm-C structure benefits from higher operating frequency and lower power consumption due to the open loop operation of operational transconductance amplifiers (OTAs). In contrary, the active-RC and MOSFET-C configurations use local feedback around the active elements, thus need much more power consumption to operate in high frequencies. However, the open loop operation of OTAs leads to more nonlinearity in Gm-C filters and demands for highly linear OTAs [12–16].

Several circuit techniques have been presented to linearize OTAs. Adaptive biasing, resistive source degeneration with passive resistors or active counterparts, cross-coupled differential pairs, triode-mode input transistors, the techniques based on floating gate and quasi-floating gate transistors and various methods of derivative superposition are frequently used to linearize OTAs [17–25]. In some cases, two or more techniques are combined to obtain higher linearity [10,12,13,26–29]. Considering some applications like Gm-C filter, the input voltages to the Gm cells have high amplitudes and high frequencies, thus, linearity improvement would be a challenging task specially under lower supply voltages in modern sub-micron technologies. This becomes more challenging by taking into account that in most applications the linearity enhancement is required in a wide range of transconductances. Moreover, employed technique for linearization should neither increase noise and power consumption nor decrease total achievable transconductance (G_m) [10,30–33].

In this paper a highly linear OTA based on a new adaptive biasing technique is proposed that uses a fully controllable low power auxiliary circuit for injecting appropriate currents to the tail current sources of differential pair. With consuming only about

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13% of the total power consumption, the proposed adaptive biasing circuit significantly improves linearity in all tuning conditions of G_m, thanks to using two control voltages that adjust circuit for the best linearization in each OTA's G_m. A wide tunable low-pass Gm-C filter is designed using the proposed OTA. The filter is tunable from 584 kHz to 10.6 MHz, thus, covers Bluetooth, cdma2000, WCDMA, UMTS and WLAN (IEEE 802.11a/g) standards.

The rest of the paper is organized as follows. The principle of adaptive biasing technique is presented in Section 2. The proposed adaptive biasing circuit and the linear tunable OTA are given in Section 3. The Gm-C filter is presented in Section 4. Simulation results are shown in Section 5 and Section 6 concludes the paper.

2. Principle of adaptive biasing based linearization

A differential pair with tail current source $2I_B$ is shown in Fig. 1. Considering quadratic equation for saturated MOS transistors M1 and M2, the differential output current is

$$i_{out} = i_1 - i_2 = v_{in}\sqrt{4I_B K_{1,2}\left(1 - \frac{K_{1,2}v_{in}^2}{4I_B}\right)}\,, \tag{1}$$

where $v_{in} = v_{in+} - v_{in-}$ is the differential input voltage and $K_{1,2}$ is $0.5\mu_n c_{ox}(W/L)_{1,2}$ in which all parameters have their usual meanings. According to (1), a nonlinear relation exists between the output current and the input voltage of a differential pair. Using Taylor series expansion the output current in (1) can be rewritten as

$$i_{out} = G_{m1}v_{in} - G_{m3}v_{in}^3 - G_{m5}v_{in}^5 + \ldots, \tag{2}$$

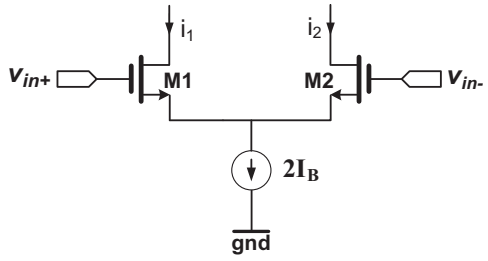

Fig. 1. Differential pair with tail current source $2I_B$.

where $G_{m1} = \sqrt{4I_B K_{1,2}}$, $G_{m3} = K_{1,2}G_{m1}/(8I_B)$ and $G_{m5} = K_{1,2}^2 G_{m1}/(128I_B^2)$. Relation (2) illustrates that in higher values of v_{in}, output current no longer keeps its linear variation versus input voltage and starts to decrease. The output current in (1) and $G_m = di_{out}/dv_{in}$ are depicted in Fig. 2 versus v_{in} for eight values of I_B changing from 80 μA to 150 μA by the step of 10 μA. The parameters are related to 0.18−μm CMOS technology and the aspect ratio of differential pair transistors (M1 and M2 in Fig. 1) is considered to be 1. As the results in Fig. 2 show, output current loses its linearity at higher input voltages and therefore G_m does not stay constant and starts to decrease when v_{in} increases. Fig. 2 also demonstrates that higher tail bias currents result in more linear output currents and more constant G_ms.

Regarding (1), the idea of adaptive biasing based linearization is to employ a tail bias current dependent on v_{in}^2 such that the phrase inside square root would be a constant value, independent of input voltage. For this purpose, we should have

$$I_B = I_{DC} + \frac{K_{1,2}}{4}v_{in}^2, \tag{3}$$

Relation (3) gives the tail bias current that makes a linear output current for differential pair. The DC part of current (I_{DC}) should be chosen to satisfy the design requirements and the coefficient of input dependent part is proportional to the aspect ratio of differential pair transistors. This idea is intuitively shown in Fig. 2(b), where the bolded part of curves could be the G_m curve of adaptive biased differential pair. In other words, a tail bias current as (3) would compensate G_m reduction due to increasing v_{in}, thus, a flattened G_m curve would be obtained for a wide range of input voltages.

3. Proposed adaptive biasing based OTA

Fig. 3 shows the concept of using an auxiliary circuit for adaptive biasing of a source degenerated differential pair. The DC part of tail currents is created by two transistors M3 and M4, while, that part which is dependent on the quadratic input v_{in}^2 is created by controllable adaptive biasing circuit. The tail current for proper adaptive biasing of the degenerated differential pair can be

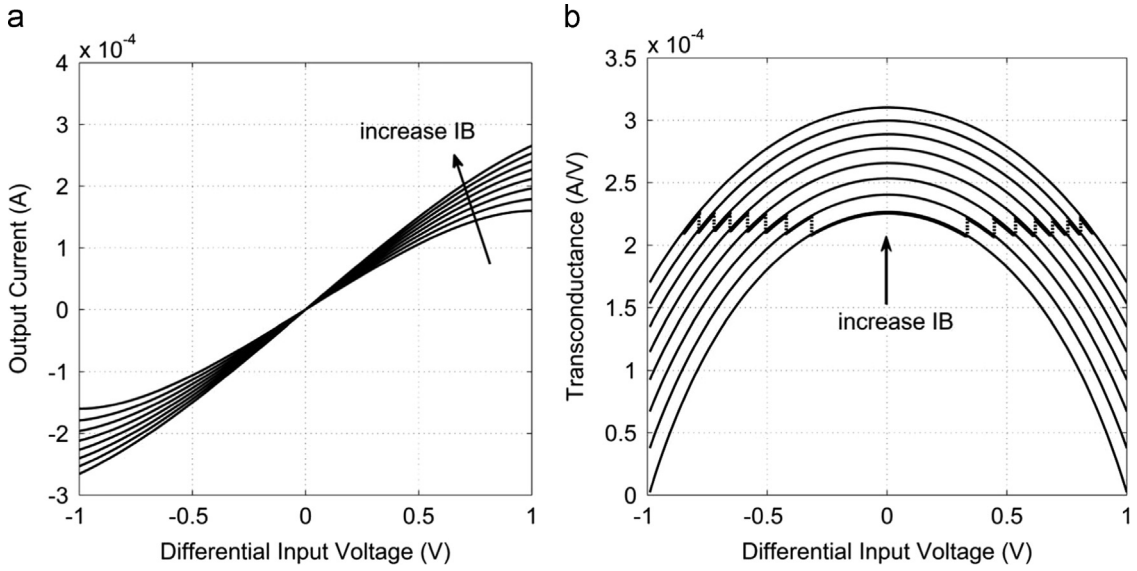

Fig. 2. Theoretical evaluation of (a) output current, (b) transconductance (G_m) of differential pair versus input voltage in various tail bias currents.