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A low power dissipation high-speed CMOS image sensor with column-parallel sigma–delta ADCs

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ABSTRACT

A 60frames/s CMOS image sensor with column-parallel inverter-based sigma–delta (ΣΔ) ADCs is proposed in this paper. In order to improve the robustness of the inverter, instead of constant power supply, two buffers are designed to provide power supply for inverters. Instead of using of an operational amplifier, an inverter-based switch-capacitor (SC) circuit is adopted to low-voltage low-power ΣΔ modulator. Detailed analysis and design optimization are provided. Due to the use of the inverter-based ΣΔ ADCs, the conversion speed is improved while reducing the area and power consumption. The proposed CMOS image sensor has been fabricated with 0.18 μm CMOS process. The measurement results show that the random noise (RN) is $7e^-_{rms}$, the pixel conversion gain is 100 μV/e^-. Since the measured full well capacity of the pixel is 25000e^-, the CMOS image sensor achieves a 71 dB dynamic range (DR). The total power consumption at 60frame/s is 58.2 mW.

1. Introduction

The market for solid-state image sensors has been experiencing explosive growth in recent years due to the increasing demands of mobile imaging, digital still and video cameras, internet-based video conferencing, surveillance and biometrics [1]. Charge coupled devices (CCDs) have been the main technology for solid-state image sensors over a few decades due to their relatively low noise level [2]. However, in recent years, complementary metal-oxide semiconductor (CMOS) image sensors have become increasingly important, because they offer the advantages of low power consumption, high-speed operation, low cost and easy system integration with on-chip circuits. Besides that, the active pixel employing pinned photodiode and double-sampling architecture are proposed to remove device variation and circuit offset that cause vertical fixed pattern noise(FPN), and greatly enhance the image quality of CMOS image sensors [3,4].

CMOS image sensors have a high degree of integration, some function modules for camera system such as pixel array, sequential circuits, ADCs, signal processing circuits can be fabricated in the same chip. At present, there are three main types of integrated ADC in CMOS image sensors: chip level ADC, column-parallel ADC and pixel level ADC.

A column-parallel ADC architecture employing a large number of parallel ADCs has become more and more popular, because it has a good trade-off among frame-rate, the number of columns, noise performance, and power consumption [5]. The architecture of ADC commonly used in column-parallel ADC CMOS image sensor includes single-slope (SS) ADC [5,6], successive-approximation register (SAR) ADC [7], cyclic ADCs [8]. Recent years, column-parallel sigma–delta (ΣΔ) ADCs have been investigated for CMOS image sensors. However, they have been applied only for low-speed image sensor with large pixel pitch due to the complexity and relatively high power consumption, and their performances are relatively worse than other ADC approaches.

In order to solve the trade-off among speed, power consumption and area of ΣΔ ADCs, an inverter-based ΣΔ modulator is proposed in [9], achieving small area, low power consumption and compatibility with low supply voltage. And the author introduced the inverter-based ΣΔ modulator to CMOS image sensor with column-parallel ADCs [10], achieving a high-speed CMOS image sensors with small area, low power consumption and improved noise performance. In this architecture, inverter is considered as a simple operational amplifier, and is applied to switched-capacitor (SC) circuits. However, the performances of inverter strongly depend on process corners, supply voltage and temperature (PVT), especially the quiescent current, bandwidth and DC operating point.

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In addition, the linear gain range of inverter is very small, a tiny change at input end will cause the gain changes greatly, which also intensifies the non-linearity of signal's setting. The above factors make it very difficult to design a good performance inverter-based ΣΔ ADC. To increase the robustness of the inverter approach, a biasing scheme which regulates the inverter bias point over the supply voltage by using an LDO is proposed in [11]. There is only one ΣΔ modulator in this chip, obviously, the extra LDO may lead to the area and power dissipation in this scheme are higher than that using a standard operational amplifier. So this scheme is more suitable for the application with a large array of ΣΔ ADCs.

In this paper, a 60frame/s CMOS image sensor with column-parallel ΣΔ ADC is presented. An inverter is used as an amplifier in SC integrator to reduce power dissipation. In order to improve the robustness of the inverter, instead of constant power supply, two buffers are designed to provide power supply for inverters, one buffer is used to sense the variation of PMOS and NOMS transistors, generating a variable voltage with process corners, the other buffer is used to provide enough driving capability and high slew rate. This paper is organized as follows. In Section 2, the architecture of the proposed image sensor is described. In Section 3, the detailed design and optimization for inverter-based ΣΔADC are presented. Section 4 provides the main circuit blocks and operation timing of the CMOS image sensor. Section 5 demonstrates the experimental results and discussion.

2. Architecture overview

Fig. 1 shows the architecture of the implemented CMOS image sensor with column-parallel ΣΔ ADC. It consists of pixel array, ΣΔ ADC array, SRAM buffer memory, column decoder, row decoder, voltage and current bias circuits, LDO and digital circuits, et al. Incremental ΣΔ ADC are well matched to the requirement of CMOS image sensor as it can provide precise high-resolution conversion with low offset and gain errors, good INL and DNL [12]. So a second-order incremental ΣΔ ADC is applied in this design. A pinned photodiode pixel as shown in Fig. 2 is used with the size of 6 μm pixel pitch. Double side allocation for readout circuits is employed, which can relax the width of one ADC to 12 μm. Because of the use of ΣΔ ADC, correlated double sampling (CDS) can be performed in digital domain, the A/D conversion is performed twice for a pixel: one for the reset level and the other for signal level, and the digital CDS is realized in the decimation filter. As the valid input range of ΣΔ ADC is proportional to the feedback voltage, so the input signal range can be adjusted by controlling the feedback voltage of ADC, and analog programmable gain amplifier (PGA) is not needed in this CMOS image sensor. The power supply for pixel array, row decoder and voltage buffer is 3.3 V. In order to reduce power dissipation, the digital blocks, including I2C bus, timing, resisters, image signal processor work at the power supply of 1.8 V, and decimation filter, SDRAM buffer memory, column decoder work at the power supply of 1.0 V.

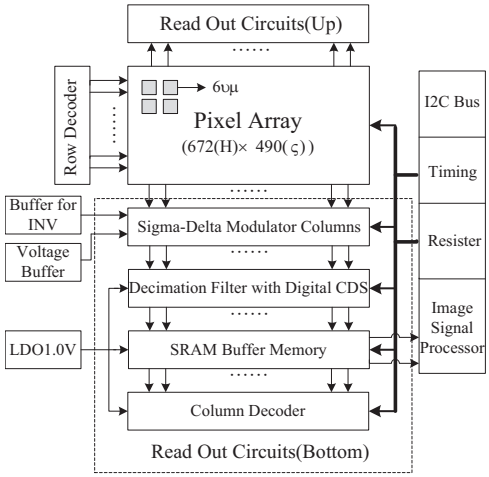

Fig. 1. Block diagram of the CMOS image sensor.

3. Implementation of the inverter-based ΣΔ ADC

3.1. Basic architecture of incremental ΣΔ modulator

The incremental ΣΔ ADC is a hybrid of Nyquist-rate dual slope converter and a ΣΔ one. The main difference to a dual-slope ADC is that the integration of input and reference is performed separately in dual-slope ADC, where in incremental one, they are alternating. The main difference to a conventional ΣΔ ADC is that the converter does not operate continuously, both the analog and digital integrators are need reset after each conversion. The architecture of incremental ΣΔ ADC is shown in Fig. 3 [12].

3.2. Operation of inverter-based SC integrator

Typical switched capacitor (SC) integrator uses an operation amplifier (OPA) with two phase clocks: sampling and integration phase. However generally speaking, OPA dissipates the most power dissipation and area of the circuit. Instead of an OPA, a logic inverter can be used as an amplifier in SC integrator as shown in Fig. 4 [9]. But there are three problems should be solved in the inverter-based SC integrator.

First of all, as an inverter has only one input, it cannot provide inherent virtual ground. When a closed loop is formed, the input node of the inverter can be expressed as

$$V_X = \frac{A}{1+A}V_{OFF} - \frac{v_{CI}}{1+A} \approx V_{OFF} \tag{1}$$

where A is the DC-gain of the inverter, v_{CI} is the voltage across integration capacitance C_I. Therefore the input of inverter is kept closed to the offset voltage of the inverter and the amount of charge transferred to C_I during ϕ_2 phase is $C_S(v_{CI} - V_{OFF})$. As V_{OFF} is

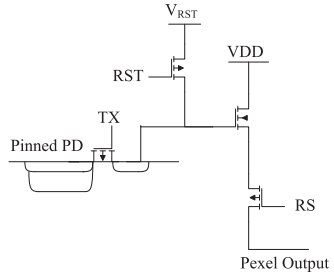

Fig. 2. Pixel schematic.

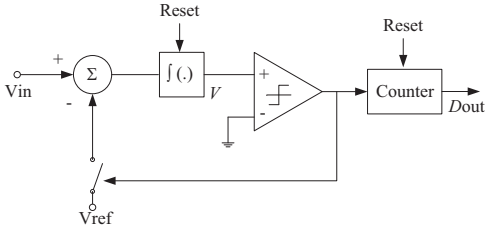

Fig. 3. Simple architecture of incremental ΣΔ ADC.