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Evaluation of layered tunnel barrier charge trapping devices for embedded non-volatile memories

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ABSTRACT

This paper presents experimental results on band gap engineered charge trapping devices for embedded non-volatile memories. Different material systems with high-*k* dielectrics and metal gates were fabricated using 193 nm lithography and the electrical evaluation was performed on 256 bits mini-arrays. The structure relies essentially on a layered tunnel ONO (oxide-nitride-oxide) barrier that replaces the tunnel oxide in conventional SONOS devices. In addition, we have implemented high-*k* dielectrics, metal gates and sealing layer in order to achieve low programming voltage and improve the data retention especially at elevated temperature. Whereas, high-*k* and metal gate systems allow low programme/erase voltages attractive for embedded non-volatile memories, the conventional band gap engineered SONOS (BE-SONOS) offers better high-temperature data retention. However, compared to a SONOS device with a standard "thick" tunnel oxide of 6 nm close to the EOT of the layered tunnel ONO barrier, it appears that BE-SONOS memories suffer from charge loss toward the channel and therefore we believe that the band gap engineered feature of the ONO barrier requires alternative materials.

1. Introduction

The scaling perspectives of floating gate memory devices are being seriously challenged. Nowadays, this successful technology which has been a standard for decades is facing fundamental problems. The tunnel oxide thickness typically close to 8 nm cannot be scaled down to preserve the data retention. As a result, programming voltages remain high and the write/erase speed does not improve [1]. In addition, the reduction of the coupling ratio and cross talk interferences are compromising the future of embedded floating gate flash technology beyond 45 nm. The non-volatile memory arena has witnessed the rise of a number of alternatives to the floating gate concept ranging from evolutionary to revolutionary devices and materials [2,3]. While being under thorough investigation in academia as well as in the semiconductor industry, none of these potential candidates has yet emerged as the ideal replacement for floating gate. It appears that the performance (speed, endurance, retention at room and high-temperature) of these new concepts [4,5] does not yet fulfill the conditions required for various applications. Among these alternatives, the band gap engineered charge-trapping concept, proposed by Likharev [6] and further advanced by Macronix has shown promising performance [7–9]. One of the major advantages of the charge trapping technology compared to floating gate is its immunity to the local defects in the tunnel oxide. Moreover, many studies proved performance gain thanks to the implementation of high-*k*/metal gates combinations [10–13]. On the other hand, reliability concerns such as read disturb, erase saturation and data retention have hindered the acceptance of charge trapping memories such as band gap engineered SONOS devices as a replacement to floating gate. Intensive theoretical as well as experimental efforts have permitted to overcome most of these challenges. However, bottlenecks especially in high-temperature data retention remain and new material systems must be investigated.

In this work, 256 bits NOR memory arrays of different band gap engineered mini-arrays were fabricated and tested with a custom made test vehicle and tester. The investigated structures are discussed with emphasis on the typical memory characteristics, i.e. program/erase (P/E) curves, endurance and data retention.

2. Band gap engineered structures

Beyond the 45 nm CMOS node, high-*k* dielectrics as well as metal gates are considered for the CMOS baseline fabrication process that could make them available for embedded integration. Among these materials, hafnium silicate ($HfSiO_x$) and hafnium aluminate ($HfAlO_x$) as well as aluminum oxide (Al_2O_3) with metal gates such

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as titanium nitride (TiN) are being considered as options [14,15]. In this work, we have assessed the potential of different material systems in combination with a band gap engineered silicon oxide/silicon nitride/silicon oxide (ONO) tunnel layer in an attempt to reduce the P/E voltage and improve the data retention.

Table 1 summarizes the devices fabricated for this study. In addition to the conventional BE-SONOS (band gap engineered silicon-oxide-silicon nitride-oxide-silicon) and BE-MANOS (band gap engineered metal-aluminum oxide-silicon nitride-oxide-silicon) introduced by Macronix [8–10], we have studied the potential of hafnium-based silicates and aluminate for the blocking oxide in combination with a HTO (High-Temperature Oxide) sealing layer (SL) and a metal gate. The purpose of the sealing layer is to increase the energy barrier seen by thermally excited electrons and therefore prevent the loss of electrons into the blocking oxide conduction bands during the write operation as well as during retention. Thanks to its wide band gap (9 eV), SiO_2 presents the appropriate offsets for both electrons and holes whereas high-*k* insulators have a narrower band gap than SiO_2. Moreover their band offsets are close to or even lower than the silicon nitride (Si_3N_4) conduction band. The sealing layer must be sufficiently thick to block direct tunneling.

3. Devices and technology

3.1. Overview

The mini-arrays presented in this work are conventional one transistor (1T) NOR arrays with memory transistors. The arrays contain 256 bits (transistors) integrated up to the metal1 level for the bit lines. The arrays are programmed and erased by direct tunneling of electrons/holes from the Si substrate. Threshold voltage (V_T) measurements are performed with 0.5 V applied on the selected bit line whereas the non-selected word and bit lines are grounded. The control gate voltage is automatically adjusted until a bit line current criterion of 5 μA is fulfilled.

3.2. Technology

The mini-arrays were fabricated using 193 nm DUV lithography for the active and gate definition. Four different structures were deposited. All have in common the layered ONO as well as 6 nm of Si_3N_4 storage medium deposited by low pressure chemical vapor deposition (LPCVD). The stacks differentiate by their blocking dielectric. After STI (shallow trench isolation) definition, the wafers are subjected to a cleaning operation. The layered ONO barrier is a critical structure that required process development in order to achieve a closed film of 3 nm LPCVD Si_3N_4, Fig. 1. Subsequently, ISSG oxide (*in situ* steamed generated) is grown on the substrate followed by a dedicated clean operation in order to modify the nature of the ISSG from hydrophobic to hydrophilic. The 3 nm tunneling Si_3N_4 of the layered tunnel ONO barrier is then deposited by LPCVD at 700 °C. Finally, a 2.5 nm HTO oxide layer is deposited in an oven at 780 °C on top of the 3 nm Si_3N_4 to form the ONO barrier. The conventional BE-SONOS devices contain a 10 nm HTO oxide for the blocking dielectric. The high-*k* based memory transistors contain either hafnium silicate ($HfSiO_x$) with 47% Si deposited by metal organic chemical vapor deposition (MOCVD) and nitrided with an *in situ* ammonia NH_3 anneal [14,15], aluminum oxide (Al2O3) or hafnium aluminate (HfAlOx) deposited by atomic layer deposition (ALD) and subsequently subjected to a post-deposition anneal in nitrogen N_2 atmosphere. The post-deposition anneal is particularly important for the Al_2O_3. In addition to the densification of the film and a shrink in thickness of approximately 2 nm, the conduction band offset of the Al_2O_3 increases upon crystallization, this property has a major impact on the performance of the Al_2O_3-based devices such as (tantalum nitride-aluminum oxide-

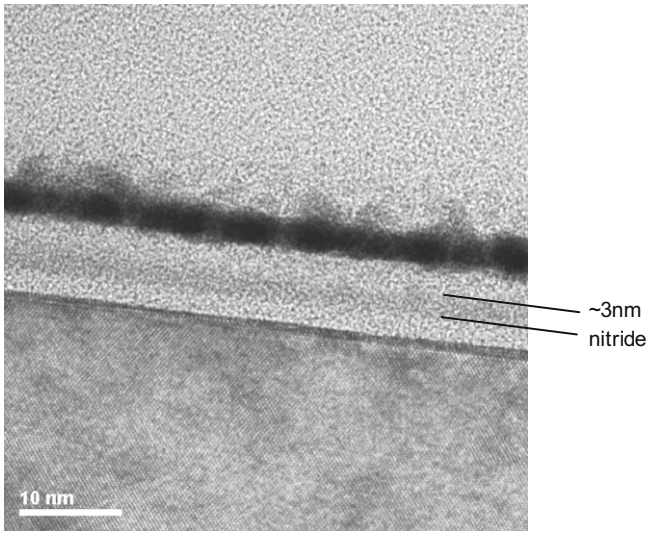

Fig. 1. TEM picture of the ultra-thin ONO barrier implemented in all band gap engineered splits. The contrast shows the 3 nm of Si_3N_4 between the tunnel ISSG oxide and the top HTO oxide of the barrier. Note that the black film has been added during the TEM sample preparation to enhance the contrast.

Table 1
Fabricated and studied band gap engineered devices. The ONO layered barrier and the trapping medium are common to all stacks.

Structure	BE-SONOS	BE-MANOS	BESHINOS with sealing layer	
Blocking dielectric and gate	Poly gate 10nm SiO_2	10nm TiN gate 17nm Al_2O_3	10nm TiN gate 20nm HfAlOx 3nm HTO	10nm TiN gate 20nm HfSiOx 3nm HTO
ONO layered barrier	6 nm Si_3N_4 2.5nm HTO 2.5nm Si_3N_4 1.5nm SiO_2 Si-bulk			