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A discrete-time amplifier based on Thin-Film Trans-Capacitors for sensor systems on foil

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ABSTRACT

Organic materials can be used to fabricate sensors for physical and chemical quantities, and also to make electronics. The integration of these two elements holds the promise to enable novel smart-sensors on foil. In this paper, we deal with the design of the first stage of a signal conditioning chain on foil: the amplifier. The poor electrical performance of organic TFTs hampers the design of complex circuits, and negatively affects the characteristics of continuous-time amplifiers. In order to improve small-signal gain and speed, a mixed discrete-time and continuous-time approach is presented in this paper for the sensor frontend. A new device, the Thin-Film Trans-Capacitor, is presented and used to build the discrete-time amplifier, while the continuous time amplifier exploits a simple traditional architecture to improve yield. Simulations of the circuit proposed show that the total gain of the sensor frontend increases of about one decade without any detrimental effect on the speed. CAD (Computer-Aided Design) simulations confirm the results of the simple mathematical model we present.

1. Introduction

Thin-Film Transistor (TFT) technologies, based on organic and metal-oxide semiconductors, are emerging as suitable solution for sensor systems on foil. This kind of technology allows the realization of large-area electronics that can be manufactured on cheap plastic foils due to the low temperatures needed for the production process [1,2]. Thanks to these features, besides mechanical flexibility [3] and high throughput [4], ultra-low cost could be achieved in mass production, enabling disposable integrated circuits. For instance, Radio-Frequency IDentification (RFID) augmented with an organic sensor could be integrated on packages at single item level to monitor the freshness of food or the storage conditions of pharmaceuticals.

The functionality of a smart sensor (Fig. 1) is obtained thanks to the integration of analog, digital and mixed signal circuits on the same plastic foil. Typically the main analog building blocks consist of an organic sensor [5] and a sensor frontend for first analog amplification and signal processing [6]. Afterwards, the analog signal is converted into a digital word [7–10] and transmitted to a base station by means of an RFID [11,12] for further processing.

This paper deals with the design of a frontend for organic sensors that allows higher gain than a single-stage topology without any detrimental effect on its speed. The final frontend exploits two Thin-Film Trans-Capacitors (TFTC) [13] in front of a continuous-time amplifier, thus implementing at the same time a sample-and-hold (S&H) function, low noise amplification, and common mode rejection.

In Section 2, we present the design and the characterization of a continuous-time fully differential amplifier. In Sections 3 and 4, we introduce the technology used to design the Thin-Film Trans-Capacitor and its design. The discrete-time fully-differential amplifier is analyzed in Section 5, and the simulated data of the combination of the two amplifiers are show in Section 6. In Section 7, some conclusions are drawn. Sections 3 to 6 expand considerably the material presented in [13].

2. A continuous-time single-stage fully-differential amplifier

Limitations imposed by the technology (as single-type TFTs, poor gain, large threshold voltage, large process parameter variations and mismatch) considerably restrict the design choices when building a voltage amplifier on foil. In our case, the technology is p-type only, thus the input pair can only be p-type (M2 and M4 in Fig. 2).

The tail current source should also be a p-type TFT and work in saturation, but unfortunately the tail source cannot be the output transistor of a current mirror (as explained in [6]). However, this function can be easily embodied by a p-type TFT used in a Zero-Vgs

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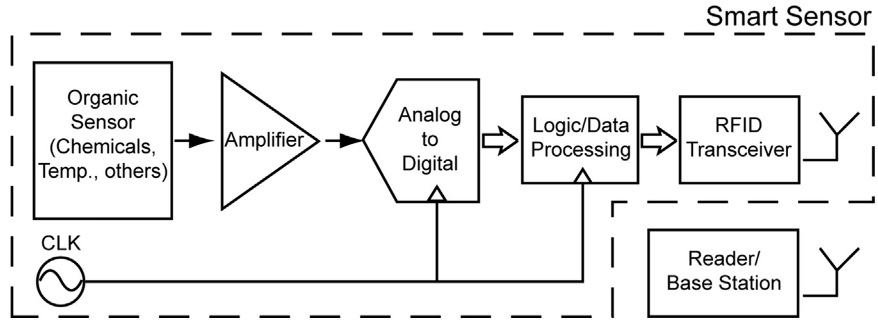

Fig. 1. Schematic of a smart sensor including an organic sensor, the analog to digital interface and the RFID transceiver to transmit the sensed data to the base station.

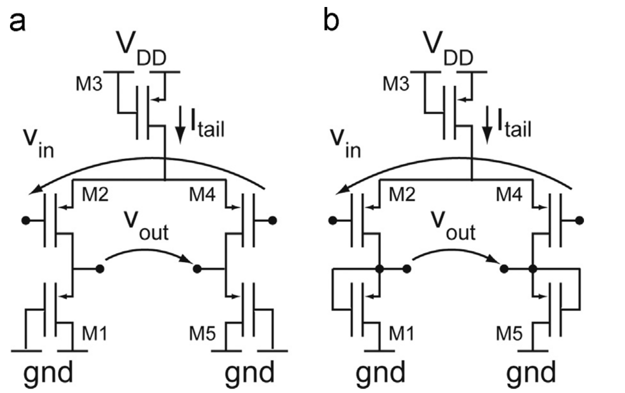

Fig. 2. Schematic of two fully-differential amplifiers exploiting (a) diode or (b) Zero-Vgs active load.

configuration (M3 in Fig. 2): this provides high output resistance and thus a relatively supply-independent bias current I_{tail}.

Neither passive loads nor self biasing solutions (e.g. current mirrors) are possible, due to the lack of resistors and complementary devices. Therefore the output loads can only be implemented with diode-connected or Zero-Vgs TFTs (M1 and M5 in Fig. 2a and b respectively).

2.1. Design and simulation

The diode load solution provides small impedance at the output node, which potentially increases the bandwidth, but also limits the gain to about 2 and keeps the output common mode very close to ground. This last effect makes very difficult the use of additional level shifters, and thus prevents the possibility to DC-couple several gain stages. Using a Zero-Vgs load the time response worsens, but higher gain can be achieved (up to 40 dB with some design effort) and the output common mode voltage can be designed to be closer to half the supply. For these reasons, Zero-Vgs loads have been preferred in this work.

In both topologies of Fig. 2, the gain of the circuit is very sensitive to input common-mode variations, thus cascading multiple amplification stages is very cumbersome or even impossible. Fig. 3 shows the output common-mode (Fig. 3a) and the gain (Fig. 3b) as a function of the input common-mode simulated for the Zero-Vgs differential amplifier of Fig. 2b. As shown in Fig. 3a, when the input common-mode $V_{CM,IN}$ is low, both the drain of M3 and the outputs are around $V_{DD}/2$, as expected. When the input common-mode $V_{CM,IN}$ becomes larger than half the supply, $V_{D,3}$ follows the inputs and the output common-mode drops, together with the bias current.

From Fig. 3b, the consequences on the gain can be observed. For a low input common-mode, the input transistors work in linear region ($|V_{DS}| \approx 0$ V and $|V_{GS} - V_T \gg 0$) and the output resistance of the amplifier drops. On the other hand, when $V_{CM,IN}$ is too high, the bias current drops drastically, the load transistors M1 and M5 exit the saturation region and provide a low output resistance. In both cases, a detrimental effect on the gain is observed.

Varying the dimension of the input devices causes a different overdrive voltage on the input TFTs (Fig. 3b), and hence it shifts the gain plateau to the right for larger widths. Increasing the width of the input devices also increases the gain due to the larger transconductance g_m. Unfortunately the difference between input and output common-mode increases too, making the design of level shifters for multi-stage DC-coupled amplifiers more complicate. Since lowering the width of the input devices also lowers the differential gain (which is already small), the final differential amplifier was designed with input device as wide as the load ones.

2.2. Layout and measurements

Fig. 4 shows the layout and the photograph of the realized circuit. Both the input TFTs and the output loads have been dimensioned with the same W/L ratio and with the same channel length. Therefore, also the number of sub-channels in the interdigitated TFTs was chosen the same.

Moreover, the tail source should provide exactly the same current provided by the two load transistors. In order to avoid systematic errors that could worsen the performance of the circuit in addition to process variations, the tail transistor was implemented using two devices in parallel, identical to the loads.

In the final layout, also two output buffers were included. These are required to perform transient measurements without affecting the circuit with external capacitive or resistive parasitics due to the measurement setup.

The tapeout includes several instances of this continuous-time amplifier, and in Fig. 5 the differential output and gain measured on 14 of them are shown.

For these measurements, the positive input was swept from ground to $V_{DD} = 20$ V, while the negative input was kept constant at 12 V. In this way, the differential output was measured and the maximum random offset could be estimated to be about 0.8 V. From these measurements also the maximum differential gain could be evaluated. Indeed, when the positive input reaches 12 V, the input common-mode is also 12 V and, according to the simulations, the maximum gain is achieved. However, the measured gain was much smaller than the simulated one, probably due to the degradation of the semiconductor mobility, and consequently to the reduced input transconductance, after a few weeks of shelf-life. Also its variability is not negligible, showing that, even after a careful design process, variations and aging strongly impact the performance of this analog circuit made with organic transistors.

3. Dual-gate organic TFT technology

Both the continuous- and the discrete-time amplifiers described here were designed with the same three metal layers TFT