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Evaluating the impact of scaling on temperature in FinFET-technology multicore processors

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ABSTRACT

Every new technology node allows higher transistor density and more complex processors to be manufactured. Unfortunately, it also means that, for the same operating conditions, power density in the chip has to increase. However, it is not obvious how this increased power density translates into temperatures in the processor, therefore in this paper we analyze the influence of technology scaling on temperature of integrated circuit manufactured in FinFET technologies. The problem is discussed based on the results of both steady-state and transient thermal simulations obtained for two modern multi-core processors manufactured in 32 nm and 22 nm technologies.

1. Introduction

The recent introduction of new transistor devices, referred to as FinFETs or Tri-Gate transistors, was mainly meant to alleviate the problem of constantly increasing leakage power in state-of-the-art integrated technologies. Unfortunately, it is very difficult to properly evaluate the impact of these recent advancements on the temperature of modern multi-core processors built with these devices. The reason is the lack of accurate block-level power models for these processors. Without such models, validated against measured data, it is impossible to obtain reliable power trace data for processor units which are absolutely indispensable for performing accurate thermal simulations for multi-core processors.

Nevertheless, in this paper the authors try to evaluate integrated circuit temperature using as benchmarks the Intel® Sandy Bridge and Ivy Bridge processors. The paper is structured as follows: Section 2 presents the organization of the floorplan in these processors and explains in detail the methodology adopted by the authors to determine the power trace data. In Section 3, results of the steady-state simulations using analytical solver based on Green's functions are presented. Section 4 describes transient thermal simulations of both processors obtained using a Hotspot thermal simulator. Conclusions and future work are presented in Section 5.

2. Power data estimation

2.1. Benchmark processors

To investigate the impact of scaling on temperatures in more detail, we analyze two Intel's quad-core architectures: Sandy Bridge [1] and Ivy Bridge [2], fabricated in 32 nm and 22 nm technology, respectively. The floorplans of these two architectures are shown in Fig. 1. In particular, two high-performance processors are analyzed: i7-3770k as an example of the Ivy Bridge architecture and i7-2700k from the Sandy Bridge family. They have the same size of L3 cache (8 MB) and nominal operating frequency (3.5 GHz) as well as comparable core voltage at the nominal frequency. Floorplans are also very similar; the only noticeable difference is that Ivy Bridge has a more advanced (and therefore a little larger) graphics unit. The dynamic and static power for the entire chip for both Sandy Bridge (SB) and Ivy Bridge (IB) processors assumed in the analyses is based on the measured power data published in [3,4]. The power measurement methodology in those articles was based on measuring the current of processors under heavy load for various values of operating frequency, temperature and core voltage values. Based on these data, we evaluated that the total power dissipated in SB and IB processors at 3.5 GHz and at 1.06 V core voltage was 100 W and 85 W respectively. Both of the above values slightly exceed the Thermal Design Power (TDP) for these processors published by Intel. This is caused by the fact that the author used a dedicated application for the so-called torture testing, which is more power demanding than the applications used for determining TDP.

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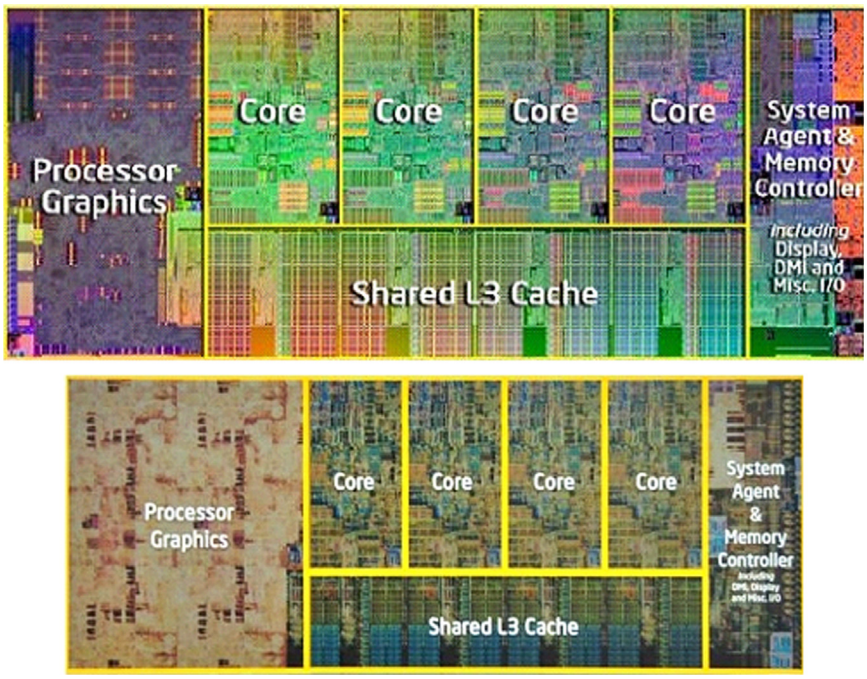

Fig. 1. Floorplans of Sandy Bridge (top) and Ivy Bridge (bottom) microprocessors resized to scale [1,2].

One interesting feature of the measurements presented in [3] and [4] is that they were performed for different values of operating frequency while maintaining the same temperature. Such an approach allows estimating the static power in the following manner: first, the total measured power is plotted against frequency. Next, by extrapolation, its component linearly dependent on frequency (dynamic power) is found. Then, we simply subtract dynamic power from total power to obtain static power. In the end, the static power was estimated at 19.9 W and 16.5 W for SB and IB, respectively.

However, for the purpose of our simulations, evaluating total power data was not enough; the data for particular processor units was needed. Given the total static and dynamic power, the power dissipation in individual processor blocks was estimated based on the several assumptions. In the first approximation, using the published SB and IB floorplans, the total dissipated power was distributed among four major units indicated in Fig. 2: 4 cores, processor graphics (PG), system agent and memory controller (SA) and the L3 cache. Furthermore, to better reflect the power density variation within a core, in the second approximation, each core was divided, as shown in the above figure, into three regions. One of these regions, CoreEX, corresponds to the core execution units and is therefore characterized by a higher power density. According to publicly available floorplans, core execution units are located in the top left corner of each core and have the area approximately equal to one-sixth of the total core area. Further details on the calculation of static and dynamic power dissipation in particular processor units are presented in the following subsections.

2.2. Static power

In the simplest approach, the static power may be distributed among processor blocks proportionally to their area. However, it would be most likely inaccurate, considering that the transistor density in regular memory-type blocks, such as the L3 cache memory, is much higher than in other blocks. Therefore, in our approach, the static power for L3 cache was estimated as being proportional to the number of transistors in cache, which can

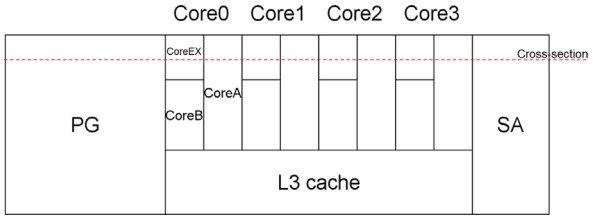

Fig. 2. A sample floor plan used in the thermal analyses. The dashed line shows a cross-section used later in the simulations..

be easily calculated knowing the cache size and assuming six-transistor (6T) cells with 10% overhead due to the tag array and logic.

Then, the remaining static power can be distributed among other units according to their area. However, since cores are typically hotter than PG and SA, a slight correction is made; for cores an additional 10% of static power is added. Note that in our approach the fact that particular processor units have different power supply values was neglected. The static power distribution was carried out identically for both SB and IB processors.

2.3. Dynamic power

Determining the correct distribution of the dynamic power is a much more complex task because it significantly varies depending on the executed application. For the measurements published in [3,4], the authors used the application designed especially for processor testing i.e. Prime95 [6]. Thus, one may suppose that the graphics unit was not extensively used and, along with the SA unit, should be the coolest part of the chip. On the other hand, the cores should be the hottest units and the dynamic power density in the Ivy Bridge core may reach 0.9 W/mm^2 and for the execution part of the core (CoreEX) even 1 W/mm^2.

Based on these power densities, we first calculated the dynamic power values for the cores for the IB processor. Then, the remaining amount of the dynamic power was distributed arbitrarily among SA, PG and L3 units. Next, the dynamic power for each unit of SB processor was calculated as a proportion between total