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High-linear, energy-efficient and area-efficient switching algorithm for high-speed SAR ADCs

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ABSTRACT

Decreasing the size of DAC capacitors is a solution to achieve high-speed and low-power successive-approximation register analog-to-digital converters (SAR ADCs). But decreasing the size of capacitors directly effects the linearity performance of converter. In this paper, the effect of capacitor mismatch on linearity performance of charge redistribution SAR ADCs is studied. According to the achieved results from this investigation, a new tri-level switching algorithm is proposed to reduce the matching requirement for capacitors in SAR ADCs. The integral non-linearity (INL) and the differential non-linearity (DNL) of the proposed scheme are reduced by factor of two over the conventional SAR ADC which is the lowest compared to the previous schemes. In addition, the switching energy of the proposed scheme is reduced by 98.02% as compared with the conventional architecture which is the most energy-efficient algorithms in comparison with the previous algorithms, too. To evaluate the proposed method an 8-bit 50 MS/s SAR ADC is designed in 0.18 um CMOS process technology. According to the obtained simulation results, the designed ADC digitizes a 25-MHz input with 48.16 dB SNDR while consuming about 589 μW from a 1.2-V supply.

1. Introduction

SAR ADC is the most popular architecture for low-power and medium-resolution applications. However the conventional SAR ADC occupies large chip area and consumes high energy owing to the large number of unit capacitors and the try-and-correct binary search for its DAC array [1]. Recently, several switching schemes have been presented to reduce the switching energy and/or chip area [2–7]. The most popular architectures like the set and down switching [2], common mode voltage-based switching (V_{cm}-based switching) [3] and tri-level switching schemes [4] as the basics for other algorithms are investigated in this paper.

The common aspect of all of the mentioned algorithms relates to sampling phase. Unlike the conventional switching algorithm, in these algorithms, the input signal is sampled on top plates of capacitors while their bottom plates are connected to reference voltages (V_{ref}, V_{cm} or ground). Therefore, sampled input is compared with zero in the first comparison cycle without any switching activity.

In the set-and-down algorithm, after determining which input terminal has higher voltage potential, related capacitor is turned down to ground to produce comparison voltage levels for the next cycle. This procedure is continued until the last bit is determined. Owing to the down transition in capacitor switching, DAC settling is improved and the number of unit capacitors is decreased by half of a conventional one which causes about 81% switching energy saving.

An alternative switching scheme is V_{cm}-based switching which benefits from using three reference voltages [3]. While the set-and-down method is more effective than the charge-recycling technique by almost a factor of 3, the V_{cm}-based switching method achieves an additional 33% reduction of consumed switching energy.

The other tri-level switching algorithm with the lowest recorded energy consumption is presented in [4]. In this technique, once the MSB is decided, the bottom plate of the capacitors which are connected to the lower voltage will be connected to V_{cm} and the other side of the capacitors remains inactivated. This means that the high-side array works, just, as a sampler and keeps the sampled input voltage and the other side acts as sampler and DAC, simultaneously. Thus the second most significant bit is determined without energy consumption. The comparison levels to extract the rest of the bits are produced by disconnecting the capacitors in the active array from V_{cm} and connecting to either reference voltage (V_{ref}) or ground, depending on the previous bit. There are two advantages for this method consisting of decreasing the switching energy consumption and reducing the number of unit capacitors. Indeed the required capacitor is decreased by a

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factor of 4 related to the conventional one (half of the capacitors in other techniques in [2,3]).

As mentioned above, the energy and area reductions in the previous methods are caused by reduction in the number of unit capacitors. But there is another way to decrease the occupied area by reducing the unit capacitor size. However the mismatch of small unit capacitors causes a non-linear effect on the ADC performance which needs some calibration mechanism to remove it. In order to achieve high-speed, high-linear SAR ADC without calibration, improvement in linearity performance of capacitor DACs is necessary to decrease the size of unit capacitors.

In the following section the effect of capacitor mismatch on linearity performance of SAR ADCs is investigated. This investigation leads to find new solution to control the non-linearity effect of capacitor mismatch. In Section 3, based on the new solution, a tri-level switching algorithm is proposed which reduces the impact of the capacitor mismatch on the linearity performance of SAR ADC. To evaluate the new switching algorithm, an 8-bit ADC is designed whose circuit details are described in Section 4. The simulation results and the conclusions are provided in Sections 5 and 6, respectively.

2. Investigation of capacitor mismatch effect on SAR ADCs

The unit capacitor in the SAR ADC capacitor array is typically limited by matching requirements. In the last conversion steps of all previous SAR ADCs, with a good approximation, there are two groups of unit capacitors which are connected to two reference voltages. This condition is modeled as capacitor array shown in Fig. 1. This capacitor array consists of two groups of unit capacitors, C_1 and C_2, connected to two different reference voltages, V_1 and V_2 the same as capacitor arrays in SAR ADCs at the final step of conversion. For calculation the non-linearity of the SAR ADC, the case of no initial charge on the array (input voltage is zero) and capacitor array with a special number (M) of unit capacitors (C_0) are considered. Each group of unit capacitor is modeled as the sum of the nominal capacitance value and an error term as shown by following equations:

$$C_1 = \alpha C_0 + \varepsilon_1, \quad \sigma_1^2 = E[\varepsilon_1^2] = \alpha\sigma_0^2 \tag{1}$$

$$C_2 = (M-\alpha)C_0 + \varepsilon_2, \quad \sigma_2^2 = E[\varepsilon_2^2] = (M-\alpha)\sigma_0^2 \tag{2}$$

where ε_1 and ε_2 are the random variables (with zero means and variances of σ_1^2 and σ_2^2) and σ_0 is the standard deviation of the unit capacitance. The output of the DAC in ideal condition ($V_{OUT,ideal}$) and with mismatch error ($V_{OUT,real}$) can be calculated by following equations:

$$V_{OUT,ideal} = \frac{\alpha C_0 V_1 + (M-\alpha)C_0 V_2}{MC_0} \tag{3}$$

$$V_{OUT,real} = \frac{(\alpha C_0 + \varepsilon_1)V_1 + ((M-\alpha)C_0 + \varepsilon_2)V_2}{MC_0 + \varepsilon_1 + \varepsilon_2} \tag{4}$$

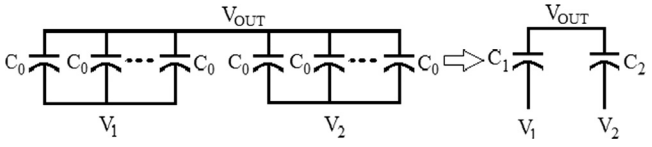

Fig. 1. A simple capacitor array to investigate the linearity performance of DACs in SAR ADCs.

According to above equations, the error voltage resulted from mismatch (V_{err}) can be obtained from the following equation:

$$V_{err} = \frac{MC_0\varepsilon_1 V_1 + MC_0\varepsilon_2 V_2 - (\varepsilon_1+\varepsilon_2)\alpha C_0 V_1 - (\varepsilon_1+\varepsilon_2)(M-\alpha)C_0 V_2}{(MC_0)(MC_0+(\varepsilon_1+\varepsilon_2))} \tag{5}$$

Compared to MC_0, $(\varepsilon_1+\varepsilon_2)$ is negligible and can be neglected in Denominator. Therefore Eq. (5) is rewritten as follows:

$$V_{err} = \frac{((M-\alpha)C_0(V_1-V_2))}{(MC_0)^2}\varepsilon_1 + \frac{(\alpha C_0(V_2-V_1))}{(MC_0)^2}\varepsilon_2 \tag{6}$$

Since unit capacitors are independent and their mismatch factors are independent and random, C_1 and C_2 are independent and their mismatch factors ε_1 and ε_2 are independent and random, also. Hence, the variance of this error can be calculated as the following equation:

$$E[V_{err}^2] = \left(\frac{((M-\alpha)C_0(V_1-V_2))}{(MC_0)^2}\right)^2 E[\varepsilon_1^2] + \left(\frac{(\alpha C_0(V_1-V_2))}{(MC_0)^2}\right)^2 E[\varepsilon_2^2]$$

$$E[V_{err}^2] = \frac{\sigma_0{}^2(V_1-V_2)^2}{M^4 C_0{}^2}((M-\alpha)^2\alpha + \alpha^2(M-\alpha)) \tag{7}$$

and the states of DAC with the maximum effect of capacitor mismatch can be illustrated by following equations:

$$\frac{dE[V_{err}^2]}{d\alpha} = \frac{\sigma_0^2(V_1-V_2)^2}{M^4C_0^2}(M^2-2M\alpha) \tag{8}$$

$$\frac{dE[V_{err}^2]}{d\alpha} = 0 \rightarrow \alpha = \frac{M}{2} \tag{9}$$

This means that the maximum mismatch effect occurs when equal numbers of unit capacitors are connected to the reference voltages. So the maximum effect of capacitor mismatch on the presented arrays in [2,3] should occur at the MSB-step($1/2V_{FS}$). And also, the worst non-linearity effect of capacitor mismatch in Ref. [4] method should appear at $1/4V_{FS}$ and $3/4V_{FS}$. It should be mentioned that calculated error by Eq. (4) relates to a capacitor array. Thus in differential SAR ADCs whose both sides are simultaneously active in switching (such as [2,3]), the error of both sides should be considered in variance calculation.

There is a very important conclusion from the above investigation to find a new possible method to decrease the effect of capacitor mismatch error. From Eqs. (7) and (9), it is understood that there are four main effective factors of the standard deviation of unit capacitor (σ_0/C_0), the number of unit capacitors, single side/differential switching algorithm and the difference between reference voltages used to produce the DAC output which can control the non-linearity effect of capacitor mismatch. The first factor refers to the process which is used for fabrication and increasing the size of unit capacitors is the only possible method to decrease this factor. The second factor of number of unit capacitor has a destructive effect and enhances the error. For the third factor, it is obvious that the limiting mismatch effect to only one side (a single array) is better than involving two arrays (for example in [4] the effect of second and third factors is compensated by each other). The fourth factor which is not considered by previous schemes refers to the difference in voltage between reference voltages. Therefore a new tri-level switching scheme is proposed which benefits from smaller difference between reference voltages. The accuracy of this claim is proved by simulation results in the following section.

3. Proposed switching algorithm

The proposed switching algorithm for a 4-bit ADC is illustrated in Fig. 2. The sampling phase and the first two conversion cycles