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Improved current drivability with back-gate bias for elevated source and drain structured FD-SOI *SiGe* MOSFET

Hoon Choi [a], Kyoho Moon [a], Chulgu Lee [a], Il Hwan Cho [b], Sang Jeen Hong [b,*]

[a] *Panel Technology Department, LG.Philips LCD Inc., 163-1, Shimi-dong, Gumi-si, Gyungsangbuk-do 730-731, Republic of Korea*
[b] *Department of Electronic Engineering, Myongji University, Yongin 449-728, Republic of Korea*

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ABSTRACT

Fully depleted (FD) silicon-on-insulator (SOI) MOSFET structure with back-gate bias is suggested for high speed and low power consumption for portable communication application. *Ni* silicide is demonstrated for improving current drivability for low power consumption by reducing series resistance in the source and drain region. Threshold voltage adjustment is also achieved through applied back-gate bias. For the formation of the buried back-gate, the selection of impurity type as well as its doping concentration is controlled. Employing back-gate bias for FD-SOI NMOSFET, improved current drivability with variable threshold voltage is achieved. Short channel devices are fabricated and its electrical characteristics are obtained under various conditions.

1. Introduction

With the growing use of portable and wireless electronic systems, high-speed devices with ultra low power consumption cannot be overemphasized in current wireless communication devices. Numerous advances in the past decades have dramatically increased the performance of silicon based devices, and such development includes the *SiGe* MOSFETs and the integration of silicon CMOS circuits in BiCMOS chips for the application of wireless telecommunications [1,2]. Material research on field effect transistors (FETs) in *SiGe*/*Si* hetero-structures have been performed, and the mobility of electrons and holes in a strained *SiGe*/*Si* are found to be approximately 60% and 5%, respectively, higher than those in controlled SOI devices [3]. In addition to the silicon-on-insulator (SOI) substrate, silicon-on-sapphire (SOS) substrate has also been proposed [4]. SOS is one type of SOI substrate which gives good thermal conductivity and heat sink capability [5].

Fully depleted-SOI (FD-SOI) elevated source/drain (RSD) structure with selected epitaxial growth of *SiGe* on a SOI substrate by using ultra high vacuum-chemical vapor deposition (UHD-CVD) is suggested for the continuous scaling down of MOSFET technology beyond the 50 nm technology node [6]. FD-SOI MOSFET has presented close-to-ideal sub-threshold slope and small parasitic capacitance, which makes it attractive for low voltage and high performance applications. In addition, thinner buried oxides can provide further reduction in short channel effects (SCE) because of the stronger capacitive coupling between source/drain and substrate [7]. However, it is difficult to control the threshold voltage and the series resistance in the thin source drain extension (SDE) degrades I_{ON}.

Recently, threshold-voltage control of FD-SOI MOSFET using variable body-factor scheme has been proposed [8]. Variable body-factor is achieved by modulating the substrate depletion layer; however, a thick buried-oxide (BOX) cause small body factor and a thin BOX cause serious performance degradation due to a large parasitic capacitance. To alleviate the concerns of the control of threshold voltage, FD-SOI MOSFET structure was employed to improve the control of the threshold voltage with a back-gate bias. The suggested FD-SOI MOSFET with back-gate bias shows improved current drivability with variable threshold voltage. Section 2 presents the suggested device concept and its underlying device physics. Sections 3 and 4 describe the device fabrication procedure and the characteristics of the fabricated device, respectively. Finally, conclusion is presented in Section 5.

2. Back-gated FD-SOI MOSFET

Back-gate structure is one of the most promising candidates for deep sub-micron fully depleted (FD) silicon-on-insulator (SOI) MOSFETs because it can reduce the short channel effect (SCE) and lower off current value per unit area provided by this structure. In addition, it can provide the flexibility in threshold voltage control.

Consider an SOI NMOSFET with N^+-doped poly-silicon gate. When the front gate is biased at its threshold voltage, an electron

* Corresponding author. Tel.: +82 31 3306374; fax: +82 31 332 2226.
E-mail address: samhong@mju.ac.kr (S.J. Hong).

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inversion layer is formed at the surface of the silicon thin-film, and the n-channel is formed for the device turn on. In the mean time, if the bulk-substrate is negatively biased, the surface of the p-type substrate under the buried oxide may also be depleted and only the ionized space charge N_A^- is left. An electron inversion layer may also exist at the back substrate surface and another inversion layer under the buried oxide can be formed. The back-gate bias affects the generation of the front channel in the silicon thin-film, and this is nominally defined as the body effect of the SOI NMOSFET device.

The proposed FD-SOI CMOS device structure employing elevated source and drain is shown in Fig. 1. During the back-gate formation, impurities can reside inside of BOX layer, and this can affect on device characteristics, such as threshold voltage, SEC, and carrier mobility. In the case of NMOS back-gate formation, implanted phosphorus in BOX disturbs the suppression of SCE due to the degradation of capacitive coupling effect between source/drain and substrate. For PMOS, the concentration of the implanted boron also may cause the threshold voltage shift and the degradation of carrier mobility. To achieve shallow junction depth with low sheet resistance, the doping concentration of the back-gate is desired to be large enough. Due to the trade-off between performance improvement and degradation, it is desired that the doping concentration of the back-gate is lower than $1 \times 10^{16}/cm^3$ and higher than $1 \times 10^{18}/cm^3$ for the SOI layer and the back-gate, respectively. This recommendation is useful for the suppression of threshold voltage shift and short channel effect of FD-SOI MOSFET, the control of doping process for the back-gate formation is crucial fabrication-wise.

Before performing any further device fabrication, it was demonstrated that how the doping profile of phosphorus affects SOI wafer. We have implanted both boron and phosphorus using ion implantation method. Then, annealing was followed in two ways; furnace annealing at 1000 °C for 30 min and rapid thermal annealing 1000 °C for 5 min in argon atmosphere. Doping profiles were investigated through SIMS, and the doping concentrations at the BOX layer were turned out to be in the order of $10^{16}/cm^3$ and at gate area were in the order of $10^{20}/cm^3$. The measured SIMS profiles at as implanted, furnace annealed, and RTA were compared in Fig. 2. As a result, it is believed that back gate formation process with ion implantation and furnace annealing is available because boron and phosphorus concentration in substrate for using as back gate is satisfied.

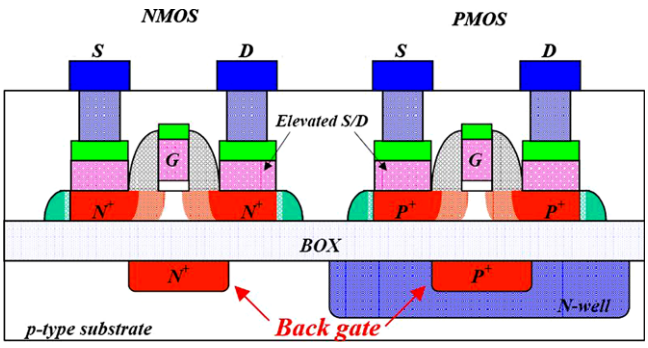

Fig. 1. A cross sectional diagram of FD-SOI CMOS with back-gate.

3. Device fabrication

Compared to conventional bulk silicon devices, fully depleted (FD) silicon-on-insulator (SOI) MOSFET has its advantages of immunity to floating effect, good sub-threshold characteristics, and suppression of short channel effect. In order to enhance the performance of the FD-SOI MOSFET, we have fabricated FD-SOI NMOS with elevated source and drain. The suggested device has very narrow junction depth underneath the BOX layer with phosphorus, and elevated source and drain (ESD) can reduce parasitic series resistance and short channel effect (SEC) in deep submicron MOSFET. The proposed device structure is presented in Fig. 3.

Boron doped SIMOX SOI substrate was prepared with two sequential cleaning steps; NH_4OH–H_2O_2–H_2O and HCl–H_2O_2–H_2O to remove organic and metal contaminants, and the implant screen oxide was grown with wet oxidation to prevent implantation damage. Active region was defined with electron beam lithography patterning and mesa-isolation was carried out using ICP-RIE. Once the active region was defined, phosphorus was implanted to form the n-type back-gate followed by electrical furnace annealing at 1000 °C for 30 min. The mesa-side surface was boron doped with ALD, and the TEOS mask was formed in the sidewall.

For the threshold voltage adjustment, $7 \times 10^{12}/cm^2$ of boron was additionally doped in the channel region with BF_2. Gate oxide was grown by wet oxidation at 800 °C, and its thickness was targeted 3.5 nm. To minimize ionic contamination between gate oxide and poly gate, 175 nm of poly gate was deposited using LPCVD. Poly gate was then patterned using electron beam lithography with TEOS hard mask, and ICP-RIE etching was performed to define gate region.

After stripping off the TEOS hard mask in gate patterning, the source and drain extension (SDE) was formed with arsenic by exposing sample in AsH_3 gas using UHV-CVD for 15 min. Fifty-five nanometres of NSG were utilized as a spacer and the *SiGe* SEG was proceeded on source and drain region for the ESD. Additionally,

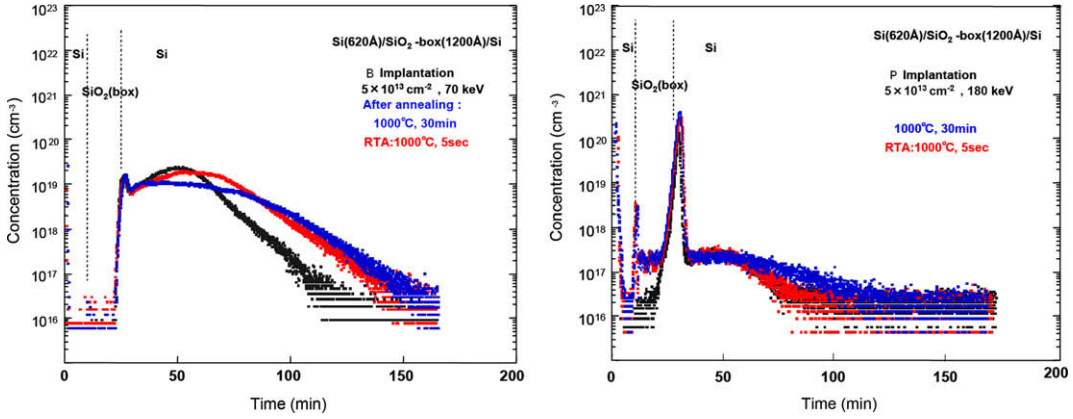

Fig. 2. SIMS profile of (a) boron for back-gate formation and (b) phosphorus for back-gate formation.