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Interfaces of high-*k* dielectrics on GaAs: Their common features and the relationship with Fermi level pinning (Invited Paper)

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1. Introduction

With the Si CMOS technology approaching its fundamental and technical limits in terms of scaling, major industrial and academic research groups have been working over the last 5-10 years on finding alternative gate dielectric and channel materials that allow continuing the scaling route as set forward by the ITRS roadmap. A lot of progress has been booked for a viable pMOS alternative, i.e., a Ge MOSFET device incorporating a high-k gate dielectric such as HfO₂ and, foremost, a clever interface passivation technique such as a Si [1] or $GeO_x(N_y)$ [2,3] interfacial layer. nMOSFET devices however turn out to be a bit more problematic. Ge seems to suffer from a rather fundamental limitation, in that it shows an energetic distribution of interface states which is rather unusual for device experts used to Si-based devices, with a high D_{it} contribution near the conduction band edge [4]. This high density of defect levels in the upper half of the bandgap, which are negatively charged and therefore counteract inversion of the channel, seems rather universal, irrespective of the passivation technique which is applied. An alternative solution might come from III/V compound semiconductors with their well-known (extremely) high electron mobilities, and a lot of research has been investigated over the last 3-5 years in these materials. The main bottleneck for the use of materials like

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ABSTRACT

Numerous metal oxides have been studied worldwide as possible high-*k* gate dielectric candidates for MOS devices on alternative semiconductor materials (Ge, III/V compounds). We will discuss thermal and plasma-enhanced atomic layer deposition (ALD) of a few materials, HfO_2 and Al_2O_3 . We will spend some attention to characteristic features of the growth process and specific growth precursors as this is known to influence strongly the quality of the layer bulk as well as the interface. Detailed electrical characterization of MOS capacitors build on such dielectric layers, before and after forming gas anneals, shows that these interface modifications can lead to a marked decrease of the smaller interface state peaks close to the edges of the bandgap, whereas the larger mid-gap peaks are barely touched. The results of atomistic modeling of the oxidation of a GaAs surface help to understand the origin of these mid-gap electronic states, which are responsible for the apparent pinning of the Fermi level.

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GaAs or In(Ga)As in MOS type of transistors has been the pinning of the Fermi level [6], which makes it difficult to invert the channel (similar to the Ge case, actually), or at least which requires quite high gate bias conditions [5] to obtain a high *I*_{on}, which are not exactly in line with the requirement of low supply voltages for low (standby) power logic circuits such as in handheld devices or wireless communication systems.

Although the problem of Fermi level pinning in III/V materials is already known for more than 20 years [6], a possible solution could come in reach thanks to the recent development of high-*k* metal oxide materials as alternative gate dielectrics in advanced Si CMOS technology for the 45 nm node such as Al₂O₃, ZrO₂, HfO₂, and other Hf-based materials. The method of choice for the deposition of such dielectric layers is atomic layer deposition (ALD), mainly because of the low deposition temperature (typically 300 °C) that still allows good quality metal oxides, among several other good reasons. One of the important things ALD process engineers learned over the years is that the starting surface on which to grow the ALD layer as well as the process conditions (mainly type of precursor and temperature) are among the determining factors for the quality of the resulting interface (D_{it} , EOT). This can easily be understood considering that any ALD growth mechanism is strongly depending on surface reactions as the chemical sites at the starting surface determine the course of the deposition process and hence the quality of the deposited layer. This has become very clear in the Si CMOS world [7 and refs. therein], and more recently,

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also in the area of Ge (p)MOS devices. Consequently, one would expect this also to be the case (and maybe even more so) for III/Vbased devices with their historically known Fermi level pinning problem. This is why we have spent quite some effort on studying the details of ALD deposition of Al₂O₃ and HfO₂ (as prototype highk materials) on GaAs including various ways of surface cleaning and preparation (Section 2). It turns out however, that obtaining a well-passivated interface in the III/V case is tougher than anticipated. In the case of Si or Ge, we have found that inserting some sort of passivation layer between the channel and the dielectric is enough, e.g., an oxide layer such as SiO₂ in the Si case or GeO₂ in the Ge case, or even a carefully controlled Si/SiO₂ combination between Ge and HfO₂ [1]. In the III/V case however, electrical characterization techniques of MIS devices that were adapted for the peculiarities of the wide-bandgap GaAs [8] teach us that these regular approaches do not quite work. To better understand the physical nature of the interface defects, we started a detailed atomistic modeling of the oxidation of GaAs surfaces, of which we will show here some results (Section 3). We will briefly discuss the results of a detailed electrical characterization of MOS devices by means of admittance spectroscopy. With the help of the ALD growth study and the insights from the atomistic modeling, we suggest a probable mechanism that helps understanding the Fermi level pinning problem (Section 4).

2. ALD deposition of Al₂O₃ and HfO₂ on GaAs

A typical ALD process consists of a consecutive series of reaction cycles, each typically involving two pulses of a precursor (for a binary compound), separated by an inert gas purge that has to prevent reactions in the gas phase (chemical vapor deposition contribution). Important aspects of the growth process are the growth per cycle (GPC), which indicates how much material grows per cycle, the growth mode, the thickness at which the growing layer closes, and the interfacial layer composition. The GPC usually is very different for the first cycle(s) (heterogeneous growth) as compared to the steady growth mode GPC (homogeneous growth). The effect of surface preparation, e.g., native oxide, wet clean and Spassivation on all these growth process aspects has been investigated for two HfO₂ processes (HfCl₄/H₂O and TDEAH/H₂O (tetrakis diethyl amino hafnium)) and for two Al₂O₃ processes (both with (CH₃)₃Al (trimethyl aluminium, TMA), but one in a thermal mode with H_2O and the other with O radicals in an O_2 plasma, plasmaenhanced ALD or PE-ALD). The growth from initial sub-monolayer coverage to continuous film has been studied by means of Rutherford back-scattering or Total X-ray reflectance fluorescence (TXRF) and XPS. Static time-of-flight secondary ion mass spectroscopy (static TOFSIMS) was used to study the growth mode: because of the very high surface sensitivity (maximum one or two atomic layers deep), this technique is well suited to measure the surface coverage after a small number of ALD cycles. Doing so for samples with an increasing number of cycles, one obtains so-called decay curves, e.g., in the case of HfO2 on GaAs, one can follow how quickly the Ga (or As) signal decays when gradually more and more of the surface is covered with HfO₂. A normal two-dimensional growth is characterized by an exponential decay with a characteristic length λ = 0.2 nm, i.e., the secondary ion escape depth [7]. A slower substrate signal decay indicates island growth.

2.1. GaAs surface preparation before ALD high-k growth

We have investigated several ways of stripping the native oxide film from the GaAs surface by wet etching [7,9]. Wet cleaning of GaAs wafers was performed in a H_2SO_4/H_2O_2 (SPM) mixture followed by 5 min etching in either diluted HCl (3.7 wt%), diluted HF (4.8 wt%), diluted HBr (4.9 wt%) or (NH₄)₂S (25 wt%) (in the last case 0.5 min dip followed by 1 min H₂O rinse), all followed by blow-drying with N₂ gun. X-ray photoelectron spectroscopy (XPS) shows the native oxide to consist of As₂O₃, As₂O₅ and Ga_2O_3 , see Fig. 1, and it is ~0.7 nm thick. None of the applied wet etchants removes the native oxide completely, although all of them do dissolve some of the GaO_x and most do dissolve some or all of the AsO_x (Table 1). The associated thickness decreases proportionally (not shown). Assignment of the small shoulder in the Ga3d spectrum in the (NH₄)₂S treated case could be difficult, as both Ga-O and Ga-S bonds show a shift of 0.7 eV compared to the bond energy of GaGa-As. Further work has shown that GaS-passivation seems to suppress re-oxidation of the oxide-free surface prepared by HCl cleaning, and the presence of chemically bonded S on the surface as As₄S₄ and Ga₂S₃ has been confirmed in As3d and S2p spectra, respectively [10].

2.2. ALD deposition of HfO₂ on GaAs

For the HfCl₄/H₂O process, we have worked with the HClcleaned surface as well as with the native oxide, left after the SPM clean. It turns out that the starting growth characteristics are quite different. The GPC of the HfCl₄/H₂O ALD on the native oxide is enhanced in the first reaction cycle (Fig. 2) with a value of 9.5 Hf/nm² which is larger than that allowed by steric hindrance assuming only ligand exchange reactions. The contribution of other reactions in an agglomeration mechanism is therefore obvious. The Hf-content increases linearly after the first reaction cycle. The TOF-SIMS ⁷¹Ga decay curve (Fig. 3) is slow for the first cycles, followed by a faster decay for thicker HfO₂ films: initially the layer grows as islands, and once the film is closed (after about 40 cycles, 1.5 nm) it grows in a more two-dimensional growth fashion. XPS measurements were performed after several weeks after the HfCl₄/H₂O ALD to check on re-oxidation of GaAs during air exposure. For samples with 2 nm HfO₂, the XPS As3d spectrum remains free of As₂O₃ and As₂O₅ peaks even after extensive air exposure. This further indicates that a 2 nm HfO₂ layer fully covers the GaAs substrate and prevents its re-oxidation in air, in agreement with TOFSIMS. Concerning the interface, a TOFSIMS depth profile indicates a rather sharp interface between HfO₂ and GaAs and no As or Ga is present in the HfO₂ layer (Fig 7 left pane). XPS indicates no interfacial layer (no AsO_x or GaO_x peaks) between GaAs and HfO_2 for HfCl₄/H₂O ALD. This implies that the native oxide, present before ALD, has been consumed by the ALD process. Thinning or complete removal of the initial oxide (the "self-cleaning effect") was reported before for other ALD processes on GaAs and InGaAs at similar temperatures [see, for example, 11,12]. It is interesting to note that the agglomeration reaction mechanism, proposed to explain the observed initial growth enhancement, also implies removal of oxygen from the starting surface by HfCl₄.

On HCl-cleaned GaAs, the Hf-content in the first HfCl₄/H₂O reaction cycle is not reproducible (values from 4.1 to 11.5 Hf/nm² are observed). This is attributed to small differences in the air exposure time between HCl clean and wafer loading, resulting in differences in the native oxide coverage of the GaAs substrate that affect the HfCl₄ reaction. Deposition of 40 reaction cycles gives a reproducible HfO₂ thickness, indicating that the effect of the starting surface on the Hf-content becomes less pronounced and the steady GPC of 1.2 Hf/nm² is reached. In contrast to the native oxide starting surface, XPS shows re-oxidation of GaAs during air exposure for HClcleaned GaAs samples with 2 nm HfO2. AR-XPS indicates the presence of AsO_x throughout the entire HfO₂ layer and even on top. This suggests that the 2 nm HfO2 layer on HCl-cleaned GaAs was not entirely closed. The TOFSIMS ⁷¹Ga decay curves confirm that there is an extensive island growth regime. Also atomic force microscopy (AFM) indicates severe problems with the HfO₂ nucleation on Download English Version:

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