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Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator

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ABSTRACT

In this paper we compare the interface trap distributions $D_{it}(E)$ of sulfur treated $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces, which underwent MOS capacitor and transistor fabrication processes. Lower interface trap densities were found close to the conduction band edge for both cases. The inversion channel MOSFET achieves high device performance despite the fact that its oxide-semiconductor interface quality is a notch below that of the MOS capacitor with optimized process.

1. Introduction

Recently inversion channel n-MOSFET has been the focus of novel high-κ/III–V research [1,2]. High performance MOSFETs have been demonstrated on InGaAs substrates with 53 percent and higher indium content, different gate stacks and sulfur surface treatments [3,4]. To further optimize the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface quality and explore its full electrical potential, MOS capacitors and transistors were made with different levels of passivation in this work. The $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitor samples received aqueous sulfur treatment prior to ALD oxide deposition and hydrogen forming gas anneals with catalytic gate metal. The MOS transistors, due to the thermal budget limit, received only the sulfur treatment. The purpose of this study is to examine and compare the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces with the baseline or optimized processes (MOS capacitor) and with the transistor fabrication process (MOSFET).

2. Device fabrication

In the MOS capacitor study, devices were fabricated on InGaAs wafers with a lattice-matched n- or p-type $In_{0.53}Ga_{0.47}As$ layer ($2 \times 10^{17}/cm^3$ doping) on InP ($1 \times 10^{18}/cm^3$ doping) substrates. The $In_{0.53}Ga_{0.47}As$ surface was treated with ammonium sulfide $(NH_4)_2S$ solution before a 10 nm Al_2O_3 film was deposited by a Pulsar^{TM} 2000 ALD system. The deposition temperature is 300 °C with water and TMA (Tri-methyl-aluminum) precursors. Palladium metal gates were then deposited via an electron beam evaporation system. A post deposition anneal with forming gas (10% H_2) was performed on these MOS capacitors to improve the corresponding interfacial quality. The combination of catalytic metal and hydrogen forming gas is to generate atomic hydrogen for further passivation. Capacitance–voltage (CV) and conductance–voltage (GV) measurements were carried out using a HP4284A LCR meter and a HP4294A impedance analyzer.

Self-aligned inversion channel n-MOSFETs were also fabricated on the same p-type $In_{0.53}Ga_{0.47}As$ on InP wafer with the same $(NH_4)_2S$ surface treatment and 10 nm ALD Al_2O_3 gate dielectric. TiW was deposited as the metal gate. For source and drain junctions, self-aligned silicon implant (50 KeV/1E15 cm^{-2}) and a 600 °C/60 s dopant activation anneal were performed. Oxide films on top of the drain and source regions were removed by a buffered oxide etch to allow the formation of n-type ohmic contacts via electron-beam deposition. Source and drain contacts were completed after the metal lift-off and 400 °C anneal. Transistor IV characteristics were measured using an Agilent 4156C transistor parameter analyzer.

3. Electrical characterization of interface trap densities

The capacitance–voltage (CV) curves of the n- and p-type samples are illustrated in Fig. 1. The measurements were performed in

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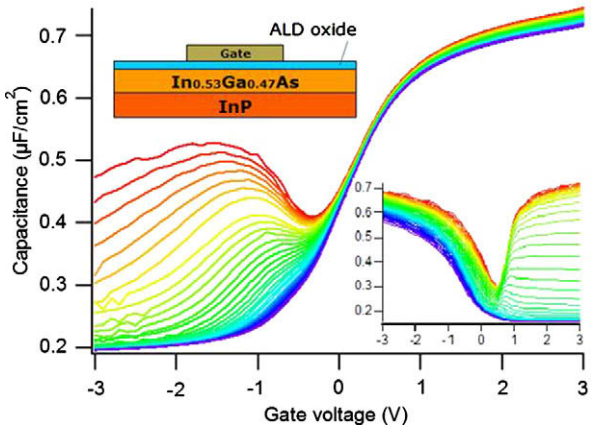

Fig. 1. Fabricated MOS capacitor structure and the CV traces of n-type MOS capacitors measured from 3 KHz to 1 MHz. Inset: p-type CV traces measured from 100 Hz to 1 MHz. Measurements were performed at room temperature without illumination.

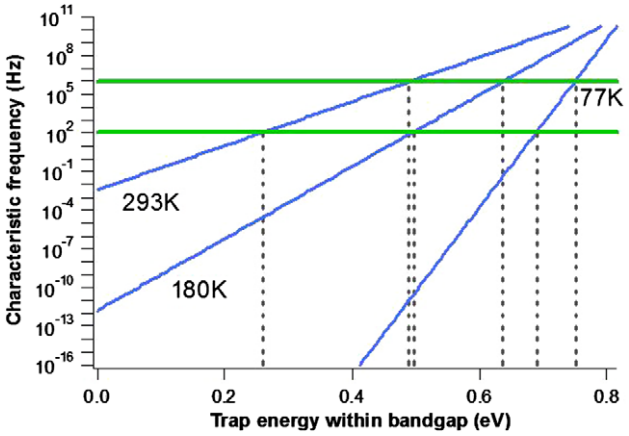

Fig. 2. The characteristic or measurement frequencies of typical CV measurements range from 100 Hz to 1 MHz. According to the charge trapping characteristics, these frequencies interact with traps within different energy windows at different temperatures. Three measurement windows at 77 K, 180 K and 293 K are illustrated for n-type $In_{0.53}Ga_{0.47}As$ substrate.

a dark ambient and up to 50 frequencies were measured between 100 Hz and 1 MHz.

To extract the interface state densities $D_{it}(E)$ across the $In_{0.53}Ga_{0.47}As$ bandgap, capacitance–voltage (CV) and conductance–voltage (GV) measurements need to be performed at different temperatures. Charge trapping characteristic equation is adopted for estimating the trap energy levels [5]. The characteristic trapping response time τ describing the time needed for a captured charge to be released by a trapping state at energy level E can be written as:

$$\tau = \frac{1}{2\pi f} = \frac{\exp(\Delta E/kT)}{\sigma \upsilon_t N} \quad (1)$$

where f is the characteristic or measurement frequency, ΔE ($E_c - E$ or $E - E_v$) is the difference between the energy level of the trap state and the majority carrier band edge, σ is the trap state interaction cross section, υ_t is the thermal velocity of the carrier and N is the density of state of the majority carrier band. By assuming certain trap interaction or capture cross section, one can relate a particular trap energy level to a measurement frequency at a specific temperature. The measurement window at room temperature, with frequencies from 100 Hz to 1 MHz, sits roughly between 240 and 480 mV above the valence band edge for an N-type $In_{0.53}Ga_{0.47}As$ substrate. At lower temperatures the measurement windows scale with the temperature and shift to the band edge, as illustrated in Fig. 2. It is estimated that the three indicated temperatures (77 K, 180 K and 293 K) together are sufficient to cover most trap energy levels of the upper half bandgap. Nonetheless, errors in estimated trap cross sections could result in fluctuations of estimated trap energy levels by ln10?kT (60 mV at room temperature) per decade of cross section variation. This leads to some uncertainty of the trap energy position.

For $In_{0.53}Ga_{0.47}As$ MOS capacitors the conductance data was obtained under the three different temperatures illustrated in Fig. 2. Interface trap densities were determined at depletion region using the well established conductance method [6]. For $In_{0.53}Ga_{0.47}As$ MOSFET the full conductance measurement setup was adopted [7]. The full conductance technique measures the transistor capacitance and conductance responses with biased gate and grounded drain, source and substrate. The MOSFET full conductance measurements were carried out at 77 K and 293 K. Both the extracted MOS capacitor and MOSFET $D_{it}(E)$ distributions are plotted in Fig. 8.

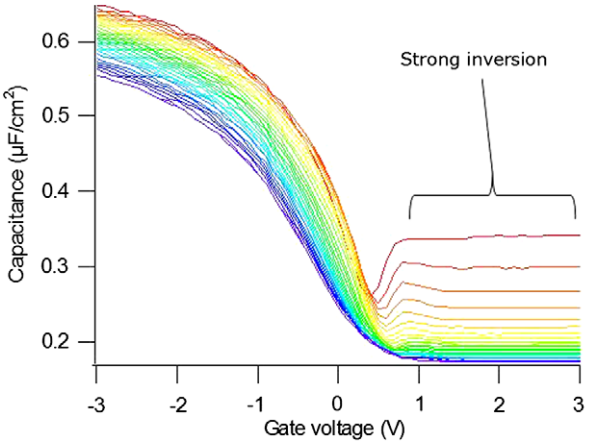

Fig. 3. CV traces of p-type MOS capacitors measured from 1 KHz to 1 MHz. The capacitance values become bias independent at strong inversion. The CV hump near 0.8 V suggests some interface trap response at weak inversion. Measurements were performed at room temperature without illumination.

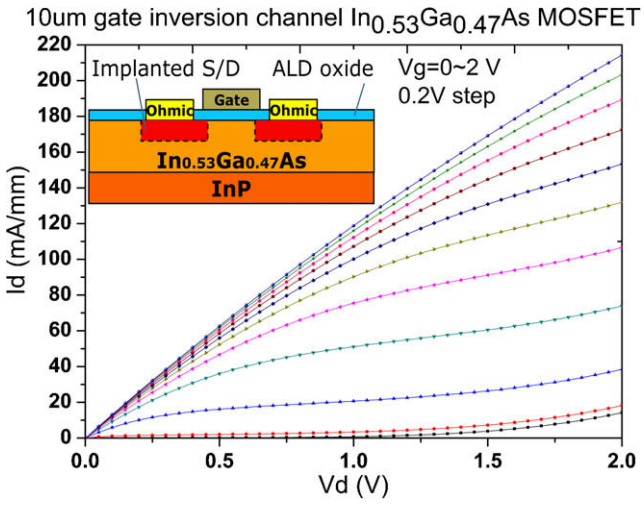

Fig. 4. I_d–V_d characteristics of 10-μm gate $In_{0.53}Ga_{0.47}As$ n-MOSFET with Al_2O_3 as gate stack. The gate is 50-μm in width. Device demonstrates drive current up to 200 mA/mm and transconductance up to 140 mS/mm.