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Opportunities and challenges for Ge CMOS – Control of interfacing field on Ge is a key (Invited Paper)

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ABSTRACT

Ge CMOS is very attractive for the post size-scaled Si-CMOS. However, we have to tackle a number of challenges with regard to materials and their interface control. In this paper, we discuss gate stack formation and source/drain engineering, as well as their implications for the performance of n- and p-MOSFETs. Because the Ge interface is significantly degraded by the GeO desorption occurring at a relatively low temperature (~500 °C), it is very hard to control Ge gate stack formation by a simple thermal budget control. In addition, strong Fermi-level pinning at the Ge/metal interface is a big problem in source/drain engineering. After discussing ways to control this desorption and Fermi-level pinning at the interface in both p-FETs and n-FETs, we discuss our current status of both electron and hole mobilities.

1. Introduction

Germanium (Ge) CMOS technologies are promising for beyond scaled Si-CMOS devices, because bulk mobilities of electron and hole in Ge are intrinsically higher than those in Si [1]. Electron mobility, however, is significantly degraded in the inversion layer of a Ge FET [2,3]. If this mobility degradation is due to the degraded Ge interface and is inherent to Ge [4], Ge could be used only in p-MOSFETs. To make Ge CMOS devices real, we therefore need to know what determines the quality of the Ge/GeO_2 interface, and understand why electron mobility is severely degraded in the inversion layer. Furthermore, in the Ge device era, high-k dielectrics will be indispensable for suppressing short channel effects and keeping the leakage current low. Thus, Ge interface should be assumed to be compatible with high-k materials.

Although source/drain engineering in addition to gate stack formation is a critical aspect of MOSFET design, it has often been neglected or even ignored in the design of new material devices. Both contact and diffused-layer resistances in the source/drain region would degrade the FET performance even if the carrier transport in the channel may be ideally ballistic. This engineering includes controls of Schottky barrier height (SBH) and dopant diffusion, solid solubility, and reverse-biased junction leakage. This is not easy because these properties are strongly related to very basic aspects of solid state physics and chemistry.

This paper first discusses Ge n- and p-FET properties with regard to gate stack formation and source/drain engineering and then demonstrates that electron mobility in Ge n-FET is about 600 cm^2/Vsec, which is close to that in Si n-FET.

2. Ge gate stack formation

High-k dielectrics on Ge are indispensable for Ge FETs. It has been reported that the interface layer between Ge and high-k dielectric film is much thinner than that between Si and a high-k dielectric film [5]. This is very beneficial, not only from the viewpoint of EOT scaling, but also with regard to the possible annihilation of imperfect properties of Ge native oxides. It should be pointed out, however, that even if high-k dielectrics are used instead of GeO_2, Ge–O bonds inevitably exist at the Ge interface, which possibly degrades the interface quality after some thermal processes [6]. We should, therefore, study both Ge/GeO_2 interface stabilization and Ge/high-k compatibility in terms of material interfacing.

2.1. Ge/GeO_2 interfacing control

The Ge/GeO_2 interface is much less stable than the Si/SiO_2 interface [7]. To overcome this inferiority of the Ge interface, nitrogen [8], silicon [9], and fluorine [10] passivations have been

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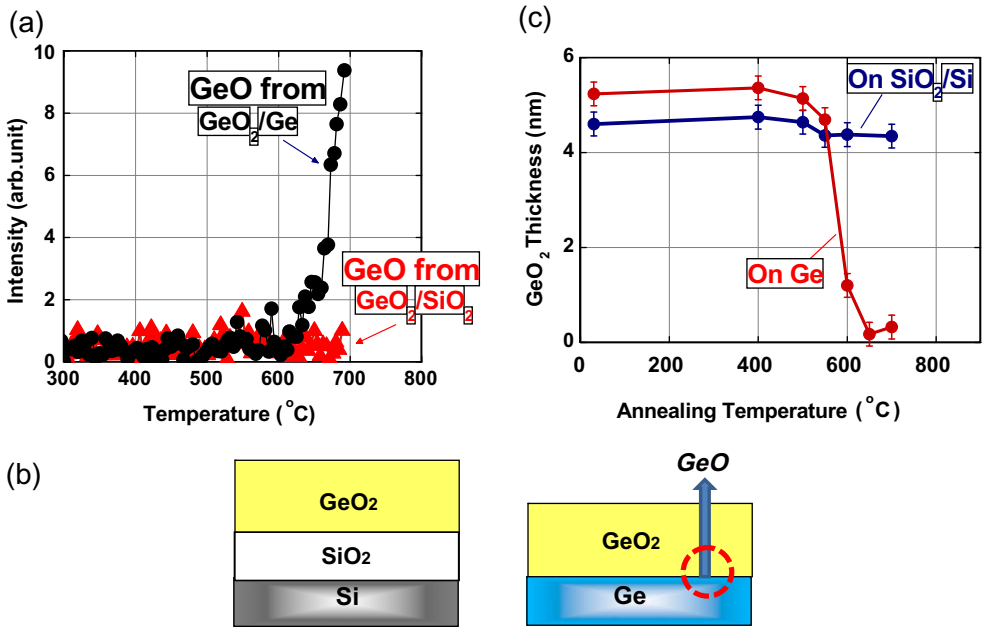

Fig. 1. (a) Intensity of GeO signal from GeO_2/Ge and GeO_2/SiO_2/Ge gate stacks as a function of the temperature in ultra-high vacuum condition. (b) GeO_2 thickness on Ge and on SiO_2/Si as a function of annealing temperature in N_2. GeO_2 thickness was measured by the spectroscopic ellipsometry. (c) Schematic view of GeO desorption in GeO_2/Ge stack.

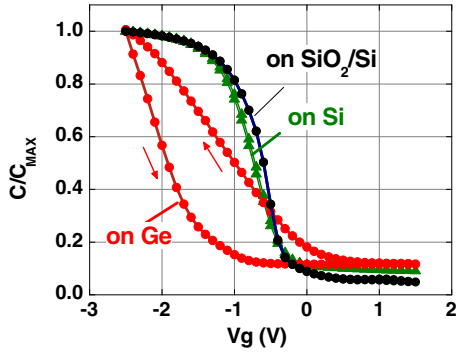

Fig. 2. Bidirectional *C–V* characteristics at 1 MHz for GeO_2/Ge, GeO_2/Si and GeO_2/SiO_2/Si gate stacks, in which GeO_2 was deposited by sputtering and then annealed in N_2 at 600 °C (Tox~10 nm). Dramatic improvements are seen in case of GeO_2/SiO_2 and GeO_2/Si gate stacks. Capacitance is normalized by the maximum accumulation capacitance.

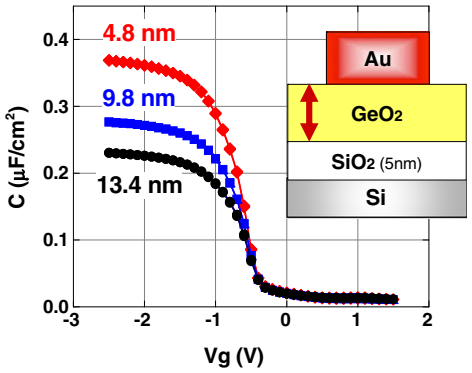

Fig. 3. Bidirectional *C–V* characteristics of GeO_2/SiO_2/Si MIS capacitors with different thicknesses of GeO_2 (4.8, 9.8 and 13.4 nm). GeO_2 was deposited by sputtering and annealed in N_2 at 600 °C. No V_{FB} shift in *C–V* characteristics is observed.

investigated. Rather than simply passivating the interface, however, we would first understand why it is degraded and then find a way to improve it thermodynamically.

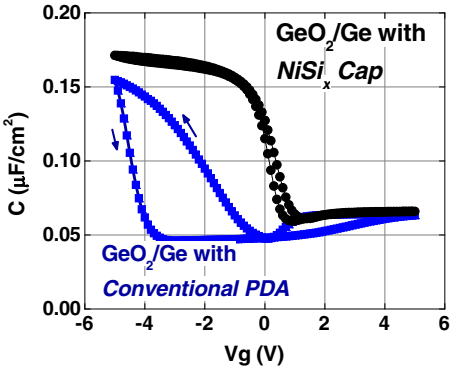

Fig. 4. Bidirectional *C–V* characteristics at 1 MHz with and without NiSi capping layer after annealing in N_2 at 600 °C (Tox~25 nm).

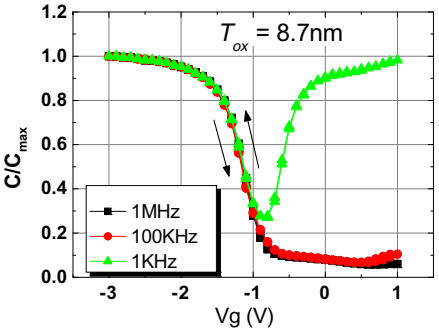

Fig. 5. Bidirectional *C–V* characteristics of high-pressure oxidized GeO_2 MIS capacitor (Tox~8.7 nm). O_2 pressure was 5×10^6 Pa at room temperature.