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Experimental evidence of suppression on oxygen vacancy formation in Hf based high-κ gate dielectrics with La incorporation

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ABSTRACT

Experimental evidence of suppression on oxygen vacancy formation in Hf based high-κ gate dielectrics with La incorporation is provided by using modified charge-pumping (CP) techniques. The original distribution of interface traps and bulk traps of pure HfO_2 and HfO_2/LaOx dielectric stack are extracted and compared by CP techniques. It is found that devices with HfO_2/LaOx dielectric stack have higher interface trap but lower bulk trap density than those with pure HfO_2. Especially, device with HfO_2/LaOx dielectric stack is highly resistant to constant voltage stress, which can be attributed to the suppression on oxygen vacancy formation in Hf based high-κ gate dielectrics with La incorporation.

1. Introduction

As the minimum feature size of CMOS devices continues to scale down below the 100 nm regime, the SiO_2 gate dielectric meets its fundamental physical limits. To reduce the large gate leakage and maintain a low equivalent oxide thickness (EOT), the gate dielectric materials with high dielectric constant (high-κ) have been proposed to replace SiO_2. Hf based high-κ gate dielectrics are one of the most promising gate dielectric for high performance field-effect transistors. However, HfO_2 high-κ gate dielectric still suffers from the low crystallization temperature [1], low channel mobility [2], and high bias temperature instability (BTI) degradation [3].

Recently, lanthanum (La) incorporation into HfO_2 has attracted much attention because of its several beneficial effects. Some researches have reported that incorporation of La into HfO_2 can raise the film crystallization temperature from 400 to 900 °C [4]. Moreover, n-MOSFETs fabricated with HfLaO gate dielectric exhibit superior electrical performances in terms of threshold voltage (V_{th}), BTI, channel electron mobility and gate leakage current compared to those fabricated with HfO_2 one. It is also reported that HfO_2 with La incorporation achieves the suppression on the oxygen vacancy formation [5]. However, there is no experimental evidence to support their calculation.

Charge-pumping (CP) technique is known as a very efficient tool to study the interface traps and bulk traps in high-κ gated MOSFETs. A profiling technique based on the variation of charge per cycle (Q_{cp}) with frequency was used to detect the border traps near the high-κ/Si interface and the interface traps [6] and to observe the phenomena and location of trap generation in the high-κ dielectric bulk while electrical stress is applied.

In this work, the distribution of interface traps and bulk traps of MOSFETs with pure HfO_2 and HfO_2/LaOx dielectric stack were extracted and compared by modified charge-pumping (CP) techniques [6,7]. It is found that the original trap distribution and the resistance against constant voltage stress (CVS) are quite different between these two MOS devices.

2. Experiment

The gate dielectrics of MOS devices studied in this work are HfO_2 and HfO_2/LaOx dielectric stack formed by an atomic layer deposition (ALD) with SiO_2 interfacial layer about 1.0 nm. The physical thicknesses are 1.5 nm for HfO_2 and 1.5/1.0 nm for HfO_2/LaOx dielectric stack, respectively. The dimension of MOS devices used in this work is $W/L = 10/0.5$ μm.

For the measurement of energy distribution of interface trap density, the rise/fall times of gate pulse are varied from 100 ns to 1 μs for frequency of 500 kHz and voltage swing is fixed at 1.2 V. Regarding the measurement of bulk trap depth profile, the rise/fall times of gate pulse are fixed at 100 ns and voltage swing is fixed at 1.2 V for frequency range of 100 Hz to 2.5 MHz. The constant voltage stress (CVS) is applied to both devices with fixed vertical electric field of 5 MV/cm to compare the stress induced trap generation in both devices.

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3. Results and discussion

Fig. 1 shows the CP current curves measured on the original, after 250 s and 500 s stressing for devices with (a) 1.5 nm HfO_2, (b) 1.5/1.0 nm HfO_2/LaOx high-κ dielectric stack, respectively. It can be seen from Fig. 1(a) that CVS causes an obvious increase in the $I_{cp,max}$ (maximum value of CP current). Although the original CP current is small, it increases almost an order after first 250 s CVS, and keeps increasing after another 250 s CVS. Results in Fig 1b show that devices with HfO_2/LaOx high-κ dielectric stack have larger CP current at origin. After CVS, the increase of CP current for devices with HfO_2/LaOx high-κ dielectric stack is smaller than that with HfO_2 one and it tends to saturate, while devices with pure HfO_2 gate dielectric does not. The original CP current of device with HfO_2/LaOx high-κ dielectric stack is larger, indicating that these devices have inferior high-κ/Si interfaces, i.e. more defects which contribute more CP current. This inferior interface could be resulted from the extra processes of forming LaOx layer. Although devices with HfO_2/LaOx high-κ dielectric stack have inferior high-κ/Si interface, the increment of $I_{cp,max}$ is smaller, indicating that Hf based high-κ gate dielectric with La incorporating does enhance the resistance against CVS.

Fig. 2 shows the energy distribution of interface trap density (N_{it}) for devices with (a) 1.5 nm HfO_2, (b) 1.5/1.0 nm HfO_2/LaOx high-κ dielectric stack, respectively. It is found from Fig. 2(a) that the N_{it} increases a lot after CVS and the energy distribution seems to move a little toward band edge. The increase of upper half of the bandgap is higher than that of lower half of the bandgap. Results in Fig 2b show that the CVS does not cause much interface trap generation on devices with HfO_2/LaOx high-κ dielectric stack. Most interestingly, the N_{it} in upper half of the bandgap is lower than that in lower half of the bandgap for devices with HfO_2/LaOx high-κ dielectric stack. For most high-κ material, the N_{it} in upper half of the bandgap is usually higher than that in lower half. This is the reason why the degradation of mobility for n-MOSFETs is usually more serious than p-MOSFETs. The unique phenomenon of HfO_2/LaOx high-κ dielectric stack might be explained by the La incorporated with Hf and O atoms to suppress the oxygen vacancy formation [5]. Hence, the electron mobility of devices with HfO_2/LaOx high-κ dielectric stack would be higher than those with pure HfO_2 gate dielectric. Furthermore, the incorporation of La is believed to reduce remote phonon scattering and increase the electron channel mobility [8] due to the modification of the atomic bonding [9,10] and reduction of trap generation.

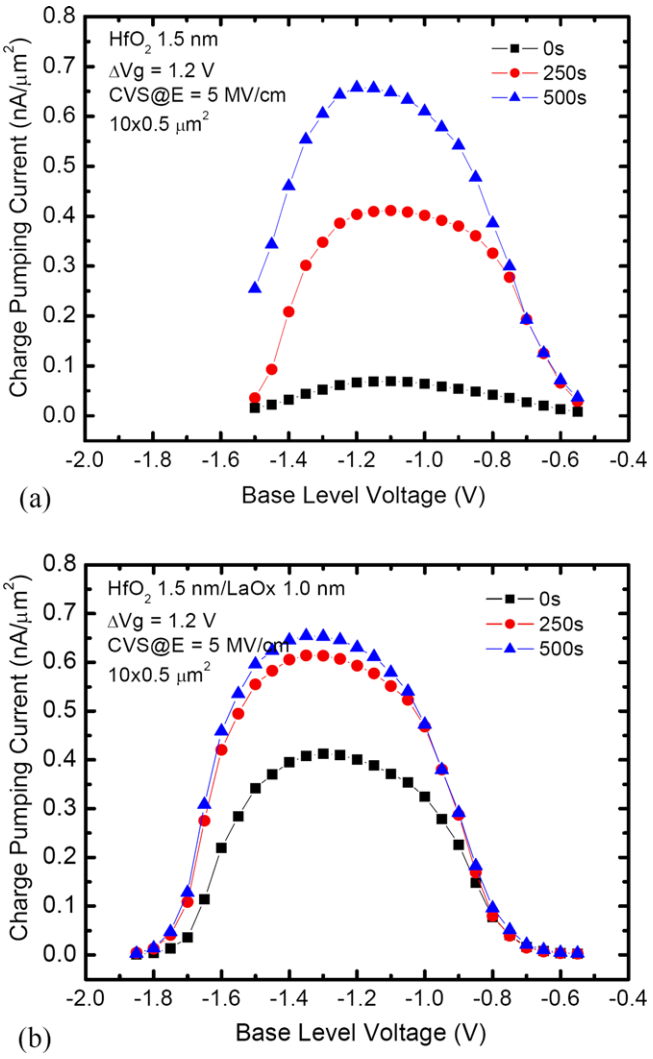

Fig. 1. CP current curves measured on the original, after 250 s and 500 s stressing for devices with (a) 1.5 nm HfO_2, (b) 1.5/1.0 nm HfO_2/LaOx high-κ dielectric stack.

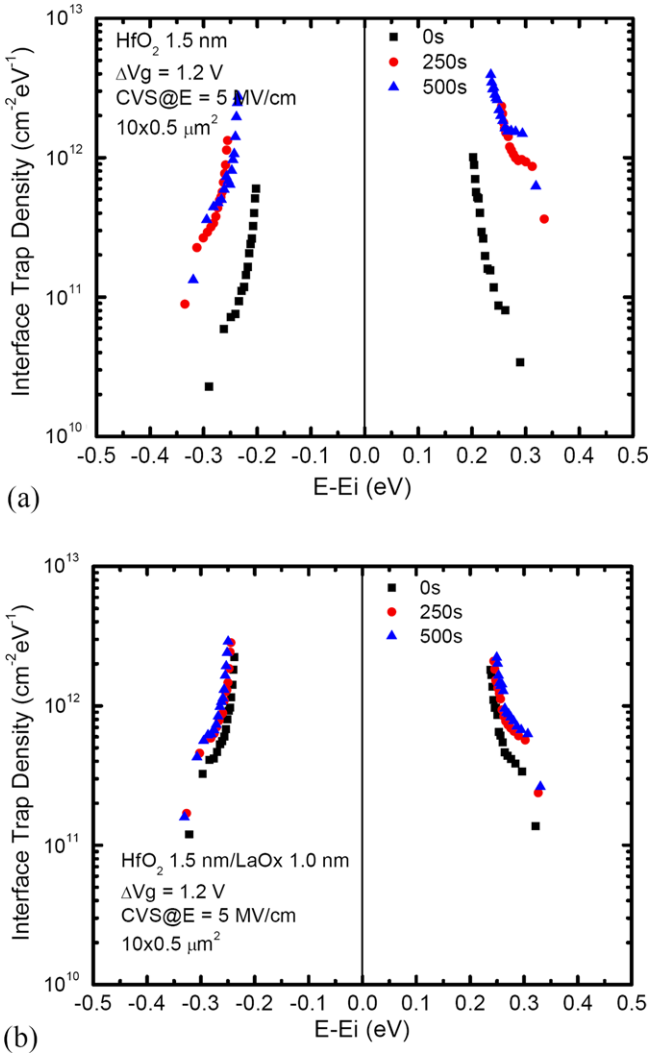

Fig. 2. Energy distribution of interface trap density (N_{it}) measured on the original and after 500 s stressing for devices with (a) 1.5 nm HfO_2, (b) 1.5/1.0 nm HfO_2/LaOx high-κ dielectric stack.