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Impact of PDA temperature on electron trap energy and spatial distributions in SiO_2/Al_2O_3 stack as the IPD in Flash memory cells

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ABSTRACT

SiO_xN_y/high-κ dielectric stack will soon replace the conventional SiO_xN_y-*based* dielectric stacks in the future generations of flash memory cells. Characterizing and reducing electron traps in the high-κ layer is an important task, as the large trap density may limit the memory retention via the trap-assisted tunneling. Since the post-deposition annealing (PDA) has great impact on the microstructure of high-κ dielectric, it is important to understand how PDA affects the properties of electron traps, such as the trap density, energy and spatial distributions. It is demonstrated in this paper that, by using a recently developed two-pulse *C–V* measurement technique, the energy and spatial distributions of electron traps throughout the SiO_2/high-κ stack can be characterized, and PDA temperatures have different impacts on traps at different energy levels and spatial locations.

1. Introduction

The scaling of the conventional SiO_xN_y-based tunnel and control dielectric layers in Flash memory technology is fast approaching its limits [1], as the increasing leakage current through thinner SiO_xN_y layers will result in a faster data loss rate. According to the ITRS Roadmap 2007 [2], this becomes the most pressing issue to be solved in floating gate Flash memory, in order to meet the charge retention and endurance requirements for future generations of Flash memory cells. Furthermore, a strong further reduction of the dielectric thickness between control and floating gates, i.e., the interpoly dielectric (IPD), is required to maintain the coupling ratio, starting from 45 to 40 nm technology generation for floating gate Flash devices [1,2]. Data retention, however, does not allow the thickness of SiO_xN_y to be further reduced.

Introduction of high-κ dielectrics as the IPD for floating gate Flash cells has been proposed as a potential solution [1,2]. Higher dielectric constant will increase the IPD capacitance without reducing its physical thickness, therefore help maintaining the coupling ratio and allow the cell size to continue down-scaling. However, the commercial application of high-κ layers in flash memory has been held back by their large electron trap density, which may limit the memory retention due to trap-assisted tunneling [1,2]. There is a pressing need for the characterization of electron traps in the high-κ layer, especially for characterizing their energy and spatial distributions, which are the essential information required for estimating the leakage current.

The existing techniques commonly used for dielectric characterization include various charge pumping (CP) [3,4], capacitance–voltage (CV) [5], conductance [6], transfer-characteristics (IV) measurements [7]. These techniques were developed mainly for characterizing the instability of MOS devices used in CMOS technologies and only have limited ability in determining the energy and spatial distribution of defects. Although these techniques allow the energy distribution of interface states to be measured within the bandgap of Si, they give little information on the energy distribution of defects in the bulk of dielectrics [4]. On the spatial distribution, some efforts [3,8,9] were made to probe into the dielectric, but none of these techniques can give a distribution throughout the dielectric. It has been demonstrated that our recently developed two-pulse *C–V* measurement technique [10] can overcome the major shortcomings of conventional measurement techniques and can probe the electron traps throughout the SiO_2/high-κ stack.

Reducing electron traps in the high-κ layer is important for the suppression of leakage current. It has been reported that PDA at different temperatures significantly changes the microstructure of high-κ layers, which may in turn affect the properties of electron traps [11]. It is possible that electron trap density can be reduced

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through optimizing post-deposition annealing (PDA) temperature. There is, however, little quantitative information available on how PDA affects electron traps, especially in terms of their energy and spatial distribution.

It is demonstrated in this paper that, by using the recently developed two-pulse *C–V* measurement technique, the energy and spatial distributions of electron traps throughout the SiO_2/high-κ can be obtained. It is observed that a decrease of PDA temperature from 1000 to 900 °C does not reduce trapping. A further reduction to 800 °C mainly reduces the electron traps at certain energy levels. PDA also has different impacts on electron traps at different spatial locations.

2. Devices

SiO_2/Al_2O_3 MOS capacitors were fabricated at IMEC using a process flow similar to that used for forming the Inter-poly Dielectric (IPD) stacks in floating gate flash memory devices. A 2 nm-thick High Temperature Oxide (HTO) was deposited as bottom layer on a *n*-type Si substrate without pn junctions. A 6 nm Al_2O_3 layer was then deposited by atomic layer chemical vapor deposition (ALCVD), followed by a conventional post deposition anneal (PDA). PDA was carried out in N_2 at 800, 900 or 1000 °C, covering the range of interest. Device fabrication was completed by deposition and etching of a TiN gate. The size of capacitors is 9×10^{-4} cm^2.

3. Measurement technique

The charge pumping technique relies on the measurement of a recombination current, which is proportional to frequency. Since detrapping time increases exponentially with the tunneling distance [12], it requires lower frequency in order to be able to probe traps situated farther from the Si substrate. The practical limitation of the frequency is typically around 100 Hz, giving a detrapping time less that 10 ms. This makes the charge pumping only suitable to probe the traps within 2 nm from the substrate [8]. The SiO_2/High-κ layers required in Flash memory cells are much thicker, usually in the range of 5–15 nm, so that the majority space is beyond the reach of even advanced CP technique.

The traditional CV/IV measurements have been used to probe charge loss at long time scales [12,13], but these measurements are too slow to characterise the defects near the interface because of fast detrapping [7,13]. To improve the measurement speed, the single pulse *I–V* technique was developed, but it did not give the energy and spatial distribution of defects [14].

In this work, we use the recently developed two-pulse *C–V* technique [10], as illustrated by Fig. 1. The waveform of the two gate pulses is shown in the inset of Fig. 1. The first pulse is used to charge the capacitor and the flat band voltage after electron trapping can be determined from its ramp-down trace. The capacitor is then discharged for a period of time, $T_{discharge}$, under a gate bias

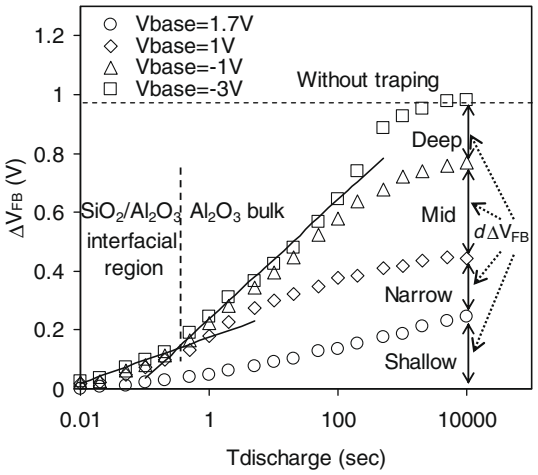

Fig. 2. The discharge induced ΔV_{FB} against discharge time at various V_{base}. The dashed horizontal line is the total trapping level.

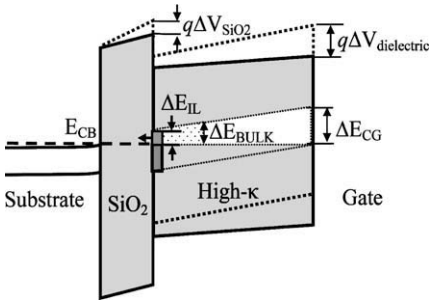

Fig. 3. Energy band diagram of the SiO_2/Al_2O_3 stack during discharge. $E_{IL} = q\Delta V_{SiO_2}$ and $E_{CG} = q\Delta V_{dielectric}$.

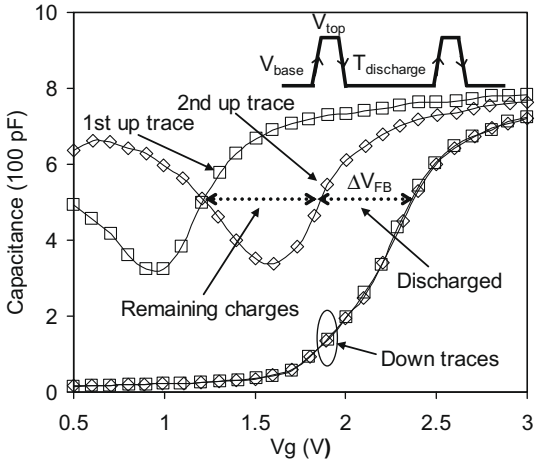

Fig. 1. Typical 2-pulse *C–V* test results. Inset shows the waveform. Test conditions are V_{top} = 5 V, T_{top} = 1 ms, $T_{discharge}$ = 10 s, and ramp slope = 10 kV/s.

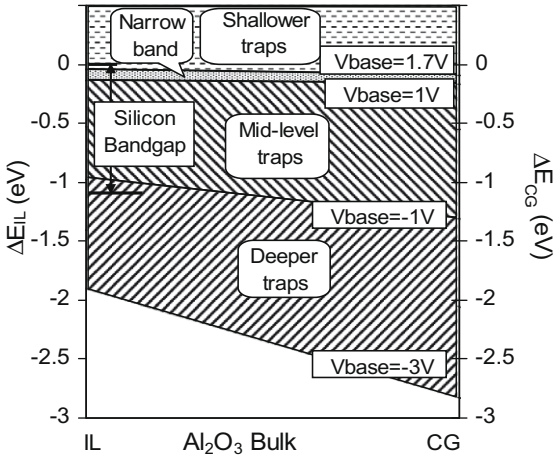

Fig. 4. Illustration of dischargeable energy bands with respect to the Si E_{CB} at the corresponding discharge bias.