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Charge retention improvement of charge-trapping type flash device by plasma immersion ion implantation

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ABSTRACT

Electrical characteristics of charge trapping-type flash devices with HfAlO charge trapping layer nitrided by plasma immersion ion implantation (PIII) technique with different implantation energies and time are studied. Utilizing Fowler–Nordheim (FN) operation, the programming speed of flash memory with charge trapping layer nitrided at low implantation energy is faster than that of control sample. The erasing speed of PIII-treated sample is slightly slower than that of control one, which might be due to the formation of silicon nitride in the tunneling oxide. The retention characteristics of all PIII-treated samples are significantly improved. Different peak locations of implanted nitrogen concentrations are formed by different implantation energies, which cause various electrical characteristics of flash devices.

1. Introduction

Polysilicon–oxide–nitride–oxide–silicon (SONOS) device is one of the most attractive charge-trapping flash memories. However, with silicon nitride layer as the charging trapping layer, over erase and the lower efficiency of charge trapping for scaling down devices remain as the main bottlenecks for SONOS device. Some high-K materials, such as HfO_2, HfAlO, and Ta_2O_5 have been proposed to replace the conventional silicon nitride layer for lowering the extra barrier during programming [1–5]. For erasing operation, the tunneling of holes would be suppressed and the phenomenon of over erase would also be avoided [1]. Moreover, owing to high-K value, gate voltage can be coupled to the tunneling oxide more efficiently to improve the characteristics of programming and erasing.

High-K materials, compared with silicon nitride layer, still have some issues, such as smaller trap density and shallow trap level [6]. Thus, the total number of trapped electrons would be smaller and the trapped electrons would escape from the traps easily. The memory window and the ability of charge retention might be worse for flash device with high-K material as trapping layer. Besides, the thermal stability of silicon nitride is better than that of high-K material. High-K material would crystallize easily during the high temperature processes of flash memory fabrication. Since leakage path is formed owing to the crystallization of high-K material, the property of charge retention is worse. How to improve the thermal stability of high-K material is also an important issue.

To improve the retention of charge trapping type flash devices, high-K material was nitrided by plasma immersion ion implantation (PIII) technique in this work. PIII technique with higher nitrogen dose and lower implantation energy, compared to conventional implantation method, can be applied to reduce the damage of implantation [7,8]. The implantation depth and concentration in very shallow region can be precisely controlled utilizing the PIII technique [9]. Effects of various implantation time/energies on operation characteristics of flash devices were studied. All samples were operated using Fowler–Nordheim (FN) mechanism, and the variations of flat band voltage were measured to investigate the characteristics of programming, erasing, and charge retention.

2. Experimental details

MOS capacitors in this work were fabricated on p-type Si (100) wafer. Fig. 1 shows the schematic cross-section of device structure. A 30 Å thick dry oxide film was formed as the tunneling oxide by a furnace. Then 60 Å thick HfAlO layer (Hf : Al = 1:2) was deposited by an atomic layer deposition (ALD) system as charge trapping layer with Al doped for the purpose of increasing the thermal stability of HfO film. Then, 150 Å thick Al_2O_3 layer was deposited as the blocking oxide. After the blocking oxide deposition, all samples were implanted by PIII technique with different implantation energies and doses. Then, a rapid thermal annealing process at 950 °C for 30 s was performed on all samples to simulate the process of

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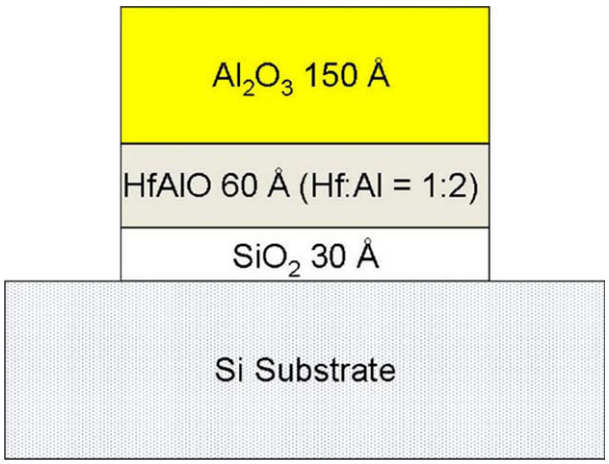

Fig. 1. Schematic cross-section of capacitor devices in this work.

Table 1
Conditions of samples treated by PIII with different energies and doses.

	N3m5keV	N2m7keV	N2m9keV	N6m5keV	N6m7keV	N6m9keV	CtrlSMP
Plasma Immersion Ion Implantation Energy							
5 keV	■			■			
7 keV		■			■		
9 keV			■			■	
Plasma Immersion Ion Implantation Time							
2 min	3 min	■	■				
6 min				■	■	■	

activation of source/drain in the fabrication processes of flash memory device. Then, all devices were completed with the following metallization processes. Conditions of samples treated by PIII with different energies and doses are shown in Table 1.

3. Results and discussion

Fig. 2 shows the depth profiles of the implanted nitrogen atoms in the device structure by simulation. The peak positions of implanted nitrogen atoms locate in HfAlO, tunneling oxide, and Si substrate surface for implantation energies of 5, 7, 9 keV, respectively. Thus, the concentration profiles of implanted nitrogen atoms can be precisely controlled by PIII with various energies.

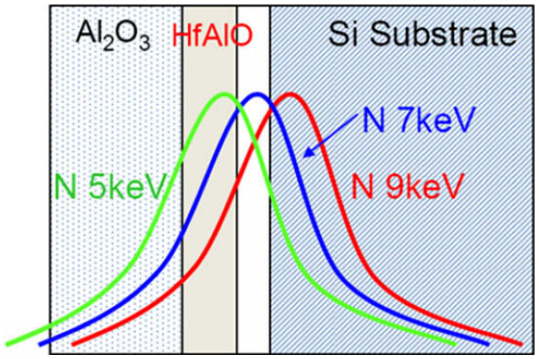

Fig. 2. Depth profiles of the implanted nitrogen atoms in the device structure by simulation.

Fig. 3a shows the programming characteristics of flash devices with different energies of PIII for 6 min. The difference of programming speed between the control sample (CtrlSMP) and N6m5 keV is small, and the programming speeds of N6m7 keV and N6m9 keV are lower than that of CtrlSMP. Because Si_3N_4 may be formed at the surface of Si substrate by ion implantation at 7 and 9 keV, the extra barrier exists while programming.

Fig. 3b shows the erasing characteristics of flash devices with different energies of PIII for 6 min. The erasing speed of N6m5 keV is slower than that of CtrlSMP. The erasing speeds of N6m7 keV and N6m9 keV samples are slightly slower than that of N6m5 keV one. Since the nitrogen atoms in trapping layer generate deep level traps, the removal of trapped electrons is harder. For 7 and 9 keV implantation energies, lots of nitrogen atoms are located at tunneling oxide and silicon nitride might be formed in the tunneling oxide.

Fig. 4 shows (a) programming and (b) erasing characteristics for flash devices with different energies of PIII for 2 or 3 min. The programming/erasing characteristics of samples treated by PIII with short time are better or comparable to CtrlSMP. The programming speeds of PIII-treated samples are higher than that of CtrlSMP because the trapping rates are larger and deeper level traps are formed by implanted nitrogen atoms [10]. The erasing speed of N3m5 keV sample is almost the same as that of CtrlSMP. For N2m7 keV and N2m9 keV samples, the erasing speeds are slightly slower than CtrlSMP owing to the formation of silicon nitride in the tunneling oxide. From the comparison of programming/erasing speeds among sample N2m7, N2m9, N6m7, and N6m9 keV, the programming/erasing characteristics of flash devices are very sensitive to the concentration of nitrogen atoms in the tunneling oxide.

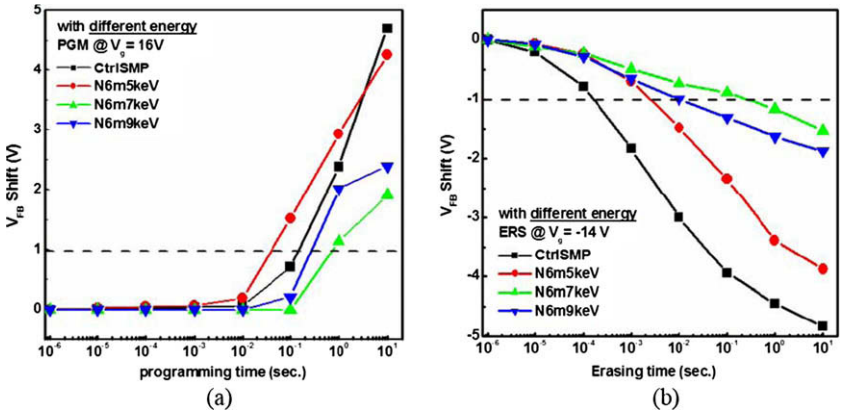

Fig. 3. (a) Programming and (b) erasing characteristics of flash devices with different energies of PIII for 6 min.