Microelectronics Journal 42 (2011) 648–660

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Design and implementation of a 0.8 V input, 84% duty cycle, variable frequency step-up converter

Mohiuddin Hafiz [a,*], Khondker Zakir Ahmed [b], Didar Islam [c], A.B.M. Harun-ur Rashid [d]

[a] Research Institute for Nanodevice and Bio Systems, Hiroshima University, Japan
[b] East West University, Dhaka, Bangladesh
[c] Power IC Limited, Dhaka, Bangladesh
[d] Bangladesh University of Engineering and Technology, Dhaka, Bangladesh

ARTICLE INFO

Article history:
Received 24 August 2010
Received in revised form
18 February 2011
Accepted 7 March 2011
Available online 2 April 2011

Keywords:
Compensation ramp
Current mode control
DC–DC converter
Duty cycle
Pulse-width modulation
Switch-mode converter

ABSTRACT

A 0.8 V input, 84% duty cycle, variable frequency CMOS DC–DC step-up converter with integrated power switches has been presented in this paper. The converter has the properties of both the current mode and hysteric control mode operations. The inductor charging time of the topology is designed to be inversely proportional to the input voltage and as a result the inductor current disturbance dies out immediately. Hence, no external components and extra I/O pins are required for the compensation of the current loop. The step-up converter has been fabricated with a standard 0.5 μm pseudo BiCMOS process. Special MOS device of threshold voltage 0.5 V and start-up circuitries enable the converter to start from a voltage as low as 0.8 V. The real time data show that the converter can boost 0.8 V to as high as 5 V, which makes it suitable for low voltage applications. The efficiency of the chip has been found over 75 % for the entire load range from 10 to 100 mA.

1. Introduction

Power management ICs, like low voltage highly efficient DC–DC step-up converters find extensive applications in electronic equipments like MP3 players, PDAs, digital still cameras, portable medical equipments, cordless phones and many other mobile hand-held devices. To make these equipments handy, the size and weight of the power modules need to be minimized [1,2]. The obvious result is to focus on the CMOS implementation of low-power converters such that the power management and the mixed-signal circuitries can be fabricated on the same die for low power applications. Among the switching regulators, voltage mode DC–DC conversion was the initial approach, but it required a large number of external components for compensation and the design of the compensation network was too involved. The obvious result was the current-mode control which requires a much simpler compensation scheme compared to its voltage-mode counterpart. Several popular modulation techniques like pulse width modulation (PWM), pulse frequency modulation (PFM) and PWM/PFM are widely used in the current mode control [3–5]. Such modulation schemes also simplify some of the design issues like over-current protection, loop dynamic responses and voltage-loop compensator design [8–10].

In a conventional current-mode design, as depicted in Fig. 1, the outer loop senses DC output voltage (FB) and delivers a control voltage to the inner loop which regulates the peak current through the power transistor on a pulse-by-pulse basis. The inner loop decides the duty cycle of the regulator depending on the sensed current through the inductor (CS) and the control signal provided by the outer loop. Such a topology, employing oscillator, is also known as fixed frequency current programmed mode (CPM) control. However, in the continuous conduction mode (CCM), a compensation using artificial ramp (SC) is needed at high duty cycle to stabilize the current loop. This issue is also known as 'sub-harmonic oscillation', as this occurs at half of the switching frequency when the converter runs above the maximum allowable duty cycle, without being compensated [11–14]. Another control topology for the DC–DC converter is the hysteric mode control, where the output voltage is controlled within a hysteric window, i.e. if the output voltage is very small, the power transistor is turned ON and if the voltage is large enough, the power transistor is turned OFF. In this control topology, no oscillator is needed and the regulation is very fast. It does not require any compensation, as well [15]. Again, the frequency variation due to the input voltage changing can be minimized by

* Corresponding author. Tel.: +81 824246265.
E-mail addresses: hafiz-mohiuddin@hiroshima-u.ac.jp (M. Hafiz), abmhrashid@eee.buet.ac.bd (A.B.M. Harun-ur Rashid).
URL: http://www.picsemi.com (D. Islam).

0026-2692/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2011.03.005

keeping the on-time of a switching cycle inversely proportional to the input voltage.

In this paper, a variable frequency, high duty cycle synchronous step-up converter combining some of the features of current mode control and hysteric control, has been developed and fabricated with a standard 0.5 μm pseudo BiCMOS process. Off-chip elements are one inductor, one capacitor and a resistive divider. No other external compensating network is needed and hence the number of I/O pins is reduced. In addition to 0.8–5 V step-up performance, the converter is well suited for other low voltage applications like stepping up 0.8 V to 2 V, 3.3 V or 1.5 V to 3.3 V, 5 V etc. with a wide range of output load suitable for electronic equipments powered by single cell battery. The topological features of the converter are addressed in Section 2. Circuit implementations of the blocks, responsible for the settlement of the loop dynamics and protection schemes are discussed in Section 3. Measured data and real time waves are shown in Section 4 to verify the functionality of the converter. Finally, the overview of the whole converter is given in Section 5.

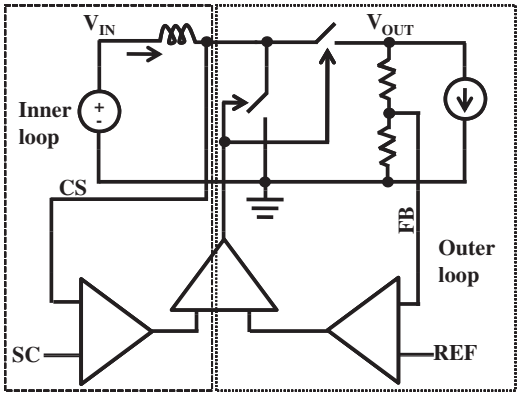

Fig. 1. The block diagram of the conventional current mode converter.

2. The topological features

The functional block diagram in Fig. 2 depicts the basic operational topology of the converter. The key elements of the current and voltage control loops are shown. Starting from the current sense amplifier, the current control loop takes combiner, time control logic and gate control logic whereas, the voltage control loop consists of the voltage sense amplifier, combiner, time control logic and gate control logic. This converter employs OFF time (Boost phase) modulation technique. The timing diagram in Fig. 3(a) explains the operational principle of both the

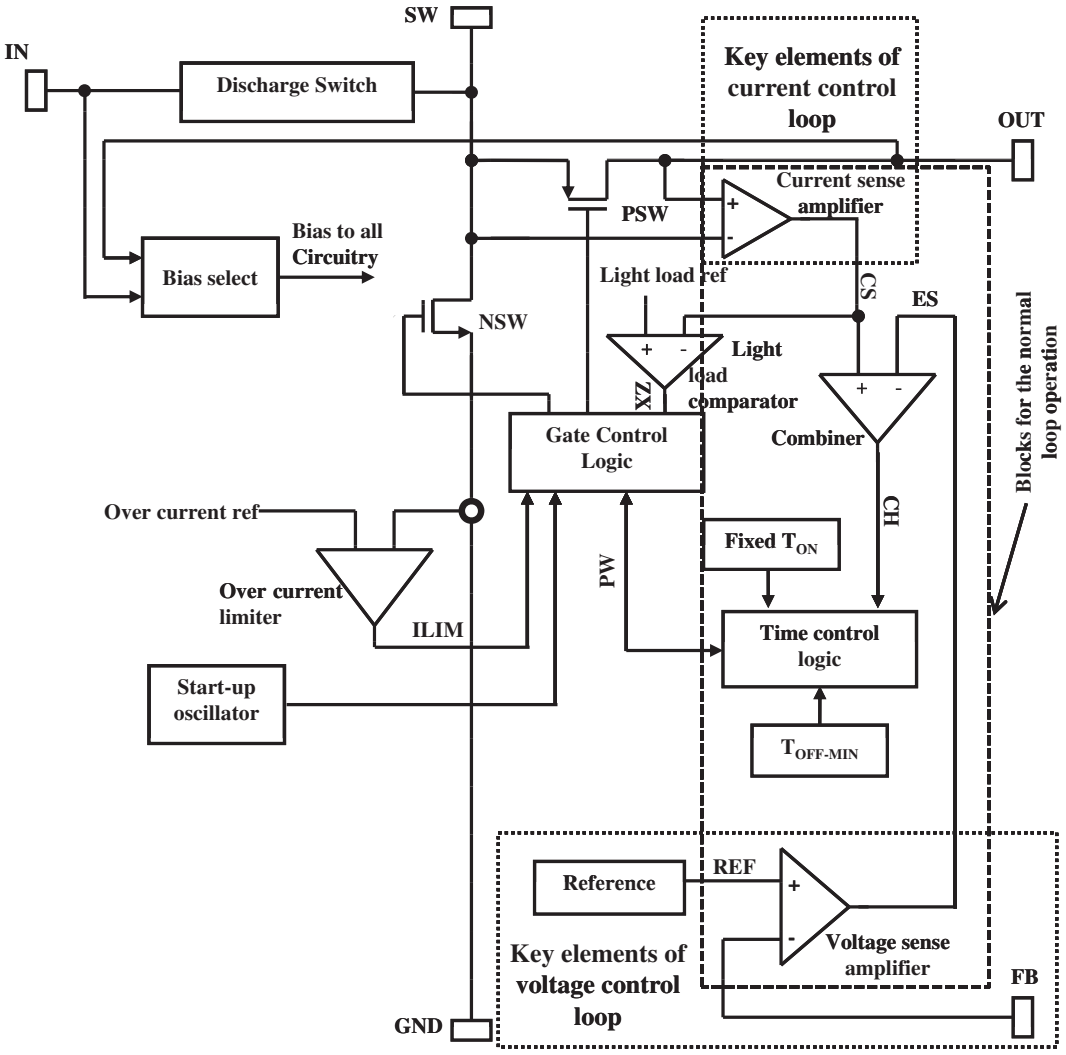

Fig. 2. The basic functional diagram of the converter.