

Degradation of current due to charge transport in top gated P3HT—PVA organic field effect transistors



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ABSTRACT

Top gate-bottom contacts transistors of Poly 3-hexylthiophene (P3HT) and cross-linked Poly Vinyl Alcohol (PVA) with different channel lengths were fabricated by standard photolithography and plasma etching. The transistors presented excellent charge mobility, high I_{ON}/I_{OFF} and temporal stability. Drain current was directly proportional to channel length. The transistors were submitted to extended current-voltage measurements and drain current degradation was observed. Reduction in transistor response was found to be related to reduction in charge carrier mobility. Drain Current as a function of the integral charge passing through the channel was investigated. The higher the integrated source – drain current that crossed the transistor, the more prominent was the degradation. The degradation followed the same pattern and persisted indefinitely. The reasons for this behavior are discussed.

1. Introduction

In recent years, conjugated polymers such as Poly (3-hexylthiophene) (P3HT) have been presented as a viable option for realizing low cost, large areas, flexible semiconductor devices [1,2]. The Organic Field Effect Transistor (OFET) structure, aside from offering a stable platform for characterizing and developing these materials [3], is being considered as the main switching element in future organic electronic devices, such as display backplanes, radio frequency identification tags, and other complementary circuits.

Charge transport has been improved considerably, through structure manipulation, so that charge carrier mobility comparable to amorphous silicon in the range of $0.1\text{--}1.0\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ have been attained [4,5]. In addition, great advances have been achieved in the environmental stability of the organic semiconductor devices. Influences of external factors, such as ambient exposure to oxygen, humidity and light were intensively analyzed [6–9]. So much has been understood that applications in the sensing industry have been considered [10,11]. Diverse techniques to minimize environmental effects have been demonstrated such as using passivation layers on top of the semiconductor or the use of top-gate/bottom contact geometries. In top-gate OFETs, the dielectric layer typically buries the organic semiconductor layer and protects it from H_2O and O_2 present in the air [12–14], but the vulnerability of organic semiconductors to organic solvents and plasma conditions used to deposit dielectric materials has

limited the use of top-gate architectures in OFETs [15].

One relevant challenge that remains to be overcome in the road to market is operational stability. Many reports have been published exploring different aspects of the OFET operation [16–18]. Instabilities are generally attributed to three main mechanisms: (1) trapping of electrical charges at the semiconductor/dielectric interface or in the semiconductor itself; (2) field-induced dipolar orientation or migration of mobile charged impurities inside the gate dielectric and (3) injection of charges into the gate dielectric from the gate electrode [19]. S. Grigorian et al. [20] attempted to evaluate the polymer during operation. A decrease in the P3HT crystallinity was reported under non-linear high current regime, whereas at low-voltage/low-current operation the structural changes were also observed. Thus, they suggested to consider this fact when controlling overall performance and stability of OFET devices.

In this paper, we present P3HT – Poly Vinyl Alcohol (PVA) top gate thin film transistors with excellent environmental stability, high mobility, and low operation voltages and off currents. Transistors with bottom contact top gate architecture and three different channel lengths were fabricated through conventional photolithography and plasma etching technique, rendering reproducible devices. Degradation of drain current response is observed using the transistors in nominal regime. The main point of our work is that the drain current, passing between source and drain is responsible for the observed behavior. The measured data as functions of the transported charge between source

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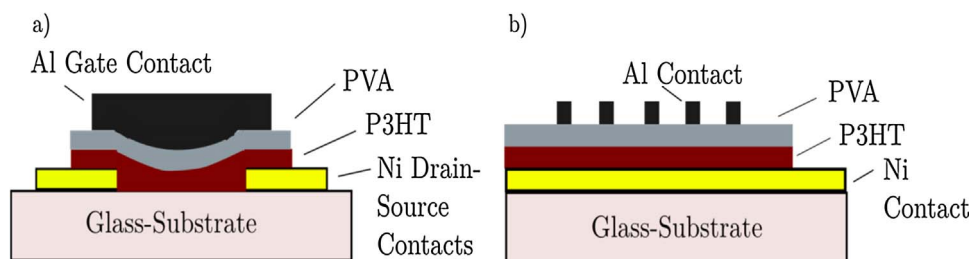


Fig. 1. Schematic diagram of (a) OFET's structures and (b) Al-PVA-P3HT-Ni capacitors.

and drain are shown, integrating the drain current. The decreasing of the drain current is related to the hole mobility decreasing.

2. Experimental

Top gate-bottom contacts OFET's with three different channel lengths were fabricated using a new photolithography process on top of glass substrates, whose structures are presented schematically in Fig. 1(a). Thin Nickel (Ni) film was deposited through sputtering (AJA Orion-8 UHV), rendering a film thickness of 150 nm. Source and drain contacts were patterned through standard photolithography followed by a wet etching step in a HNO_3 solution. These processes defined transistors with channel lengths (L) of 5, 10 and 40 μm and width (W) of 1 mm.

Regio-regular P3HT (rr-P3HT) (regioregularity > 90%) (Sigma Aldrich) dissolved in chlorobenzene (0.5 w/w%) was applied on the patterned contacts by spin coating at 1000 rpm. This film was annealed at 100 °C for 5 min to volatilize the solvent and to accommodate the polymeric chains. PVA with M_w (g/mol) in the range of 146,000–186,000 and 87–89% hydrolyzation degree (Sigma Aldrich) cross-linked with Ammonium Dichromate (ADC) was used as the gate dielectric. D.I. aqueous solution of PVA (2.5 w/w%) with ADC (0.4 w/w %) was deposited on the organic semiconductor by spin coating at 4000 rpm and annealed at 100 °C for 5 min again. These procedures generated films with thicknesses of about 50 nm for both polymers. Photoresist was deposited on the sample and the second photolithography step was performed with the mask defining the active area, which extends over the Ni contacts. After a hard baking, O_2 plasma-etching was used to cut both organic films, using the photoresist as a mask. The samples were cleaned with $\text{DI-H}_2\text{O}$ to remove any plasma process residues, and then, the photoresist was removed. Aluminum (Al) was evaporated at a base pressure of 1×10^{-6} Torr to form the top-gate electrode. After gate photolithography, the Al was etched in concentrated ortho-phosphoric acid at 50 °C.

Capacitors, schematically presented in Fig. 1(b), were fabricated in order to measure the capacitance per unit area of the PVA-P3HT structure under the gate. The layers Ni, P3HT and PVA were deposited under the same conditions as in the transistors. The deposition of the Al top contacts was performed through mechanical shadow mask rendering circle electrodes with a diameter of 200 μm .

Capacitance-voltage (C-V) measurements were performed with a precision LCR meter HP 4284A. OFETs were electrically characterized by current-voltage (I-V) measurements, using a HP4155A semiconductor parameter analyzer.

3. Results and discussion

We have measured more than 10 devices with approximately the same characteristics for each channel length and the data of the following figures are extracted from one typical device.

The capacitance vs. voltage curve at 100 kHz of the capacitor from Fig. 1(b) is shown in Fig. 2. This measurement was used to extract the gate capacitance per unit area, which is necessary for channel mobility calculations. The C-V curve is similar to a silicon MOS structure curve,

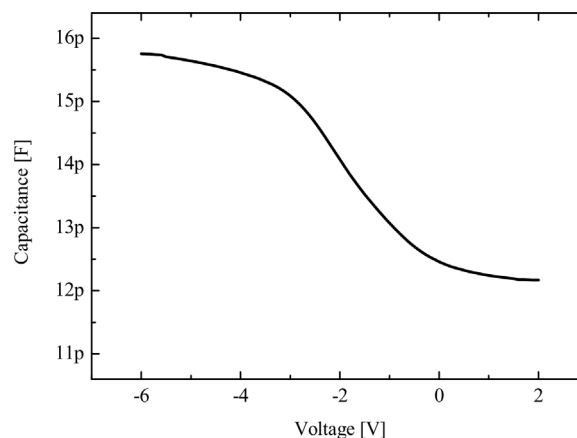


Fig. 2. 100 kHz C-V curve of the capacitor from Fig. 1(b).

but with some differences. Three well defined zones can be seen: the accumulation zone, between -6 V and -3 V; the depletion transition zone, between -3 V and zero V; and the depletion saturation zone, between zero V and 2 V. The accumulation and depletion zones are not as well saturated as accumulation and inversion regions in Si MOS structures, due to the characteristics of the hole transport in P3HT. In accumulation the positive charge of P3HT is attracted to the interface between PVA and P3HT and in this case the capacitance is increased (like in a functioning transistor with the same gate polarization). In depletion the positive charge moves away from the interface and creates the depleted P3HT capacitance, connected in series with the accumulation capacitance. In this way the total capacitance decreases. The accumulation capacitance tends to approximately 16 pF. Dividing this value by the area of the Al contact, the capacitance per unit area is calculated to be $C_i = 50 \text{ nF/cm}^2$. This value was used to extract the mobility of the transistors from the transfer curves.

The output curves for two sets of measurements of the transistors with channel lengths of 5, 10 and 40 μm are shown in Fig. 3. Each set is composed of curves that sweep source-drain voltages (V_{DS}) from zero to -8 V, changing gate-source voltage (V_{GS}) with a step of -0.1 V from zero to -6 V. The second set of measurements was carried out approximately 15 min after the first one. Although each measurement set comprises of 61 curves, for the sake of clarity only 10 curves per set are presented. Source-drain current (I_{DS}) is higher for transistors with shorter channels, in accordance with data previously reported for other organic semiconductors [20,21].

For channel length of 5 μm , the source-drain current reaches approximately 7 μA at a gate voltage of -5 V. This maximum I_{DS} is 7 times higher than the maximum I_{DS} obtained for transistors with channel length of 40 μm , which is close to the ratio between these channel lengths of 8. It follows the Shockley model and the ratio of 7 suggests that the contact resistance is much less than channel resistance, which is in accordance with other results obtained for staggered OFETs [21,22].

Table 1 presents the characteristics of the transistors with different channel lengths based on the results from the first and second

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